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FORM PTO-1390 U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER

62758-012

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U.S. APPLIC. NO. (if known, see 37 CFR 1.5)

09/914681

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/01400	March 19, 1999	March 19, 1999

TITLE OF INVENTION

DISPLAY AND IMAGE DISPLAYING METHOD

APPLICANT(S) FOR DO/EO/US

Akihiko KOUGAMI et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendment has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information.
    1. International Search Report prepared by JPO.
    2. Front page of Published International Application.

20277

PATENT TRADEMARK OFFICE

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U.S. APPLIC. NO. (if known, see 37 CFR 1.50)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/914681	PCT/JP99/01400	62758-012

	CALCULATIONS	PTO USE ONLY
17. ☒ The following fees are submitted:		
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	27 -20 =	7	x $18.00	$ 486.00	
Independent Claims	- -3 =		x $80.00	$	
Multiple dependent claim(s) (if applicable)			+ $270.00	$ 270.00	
TOTAL OF ABOVE CALCULATIONS =				$ 1,616.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 1,616.00	
Processing fee of $130.00 for furnishing the English translation later than the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 1,616.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 1,656.00	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 500417 in the amount of $ 1,656.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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BASED ON FORM PTO-1390 (Rev. 5-93)

DESCRIPTION

DISPLAY APPARATUS AND VIDEO DISPLAY METHOD

TECHNICAL FIELD

The present invention relates to a display apparatus, such as a plasma display device or the like, and in particular relates to a display technology, being suitable for use in a multi-sub field method for realizing display of high brightness, high definition and high gradation.

BACKGROUND ART

The display apparatus, such as the plasma display device or the like, are expected to spread out widely into various uses or purposes, in future, including a data display device of a personal computer or the like, and a display device for use of a game machine, etc., other than the video display device of a television apparatus. Specifications required corresponding to those various uses or purposes are various, too. For example, for use in the television apparatus, in particular for HDTV (High Definition TV), there are required the line number of 1,000 or more in the resolution, and 500 cd/m^2 or more at the peak brightness, etc. It is, also, necessary to reduce pseudo-contour obstruction, which is distinctive of the display of moving picture on the plasma display device. On the contrary to this, for the television screen is allowed the interlaced display. On a while, the requirements for the data display are, for example, the line number of about 800 in the resolution, and about 200 cd/m^2 for the brightness, and also, since it is mainly used for display of still picture or video, there

is not so much necessity of reducing the pseudo-contour, etc., thus, the specifications required is rather generous than those for the television apparatus. However, in the case of this data display, since a line flicker stands out easily, the progressive display is carried out. In this manner the specifications required for the display are different from and various depending upon the uses or purposes thereof in recent years, however such a display is desirous that it can be used in various manner by one (1) set of display device, in particular, being applicable to multimedia, for example, i.e., the display being applicable to both the television apparatus and the data display by one(1) set thereof.

However, at the present, there cannot be obtained the display, which fully satisfies those specifications required. For example, in the case of the plasma display being available at present, in particular for the use of a television apparatus, the line number is 480 in the resolution, and the brightness is 300 cd/m^2, and measures are still not sufficient against the pseudo-contour. Every one of hose three (3) properties, i.e., the resolution, the brightness, or the pseudo-contour, must be improved within the time period of one (1) field.

Also, with the television apparatus, requirement is made much more for high contrast, and for that purpose, light emission must be suppressed as far as possible when displaying black on the display screen. For example, with an AC type plasma display apparatus available at the present, it is designed so that a pilot burner discharge is conducted, therefore it is common to apply a driving method of all write-in or all erase. With this method, in which write-in operation is conducted once, upon all over the cells (i.e., all write-in) before conducting address discharge, i.e., selective write-in depending upon information, and next, wall electric charge written into all the cells is floated in a space within of each of the cells, thereby erasing it by neutralization of ion and electron (i.e., all erase), the operation of all write-in or all-erase resets the wall electric charge of

information, which was already written into, and at the same time, accelerates rising-up of discharge of address discharge with using the spatial electric charge remained only a little therein, by the all-erase (i.e., so-called a pilot light), thereby enabling the drive with low voltage. However, with this all write-in or all-erase method, discharges occur even when displaying black irrespective of information of display video, then the contrast is deteriorated due to this light emission. For this reason, a technology was proposed, wherein the all write-in or all-erase are conducted only one (1) time per one (1) field, or more or less, but not all the sub-fields within one (1) field, thereby obtaining high contrast screen. With this proposed technology, since the pilot light comes to be small in the effect thereof, there may occurs a case where the address discharge of the sub-field operates erroneously, though it should be conducted at a time point separate from that when a pulse for the all write-in or all-erase is applied to. For obtaining the high contrast screen without changing discharge condition, there are proposed technologies of bringing boundary portions of the cells on a panel into back color, and attaching a filter in front surface of the panel, and so on.

On the plasma display panel, the high definition screen can be obtained by making cell pitch fine and the number of display cells large, however in a case where the screen is constant in sizes thereof, an increase in the number of the display cells makes volume or sizes of the cell small, therefore it may occurs problems, such as a rise-up of the discharge voltage, and/or a fall-down of light emission efficiency. Relating to such the high definition of the screen, a technology of small-sizing boundary portions of the cells, or of utilizing those boundary portions aggressively for the display is disclosed in Japanese Patent Laying-Open No. Hei 9-160525 (1997), for example.

For the purpose of reduction of the pseudo-contour obstruction, various technologies were proposed for measures against thereof, up to now. A reason of generating the

pseudo-contour is based on plural numbers of the sub-fields, which form the field in a manner of time-sharing, and it is caused by generation of unevenness in brightness pattern on the retina of an eyeball due to movement of visual axis of an observer. In the phenomenon, when the observer follows her/his visual axis on a part, which gradually changes the gradation thereof, and if it moves on the screen, a profile or contour-like noise (i.e., the pseudo-contour) of high brightness or low brightness can be observed in a certain portion thereof. For reducing this pseudo-profile obstruction, there are methods of changing the alignment order of the sub-fields, or shortening all the sub-fields within one (1) field, or scattering the light emitting sub-fields, thereby dispersing the pseudo-contour noises over the pixels on the screen, so as not to be distinctive. A technology relating thereto is disclosed, for example, in Japanese Patent Laying-Open No. Hei 4-211294 (1992), in which the total sub-field is shorten within one (1) field, and a period more than a half (1/2) of that one field is made to be a suspension field, thereby to reduce the pseudo-contour.

Also, a method of address/display separation is applied into the AC type plasma display device. According to this method, within one (1) sub-field, an address period for forming the wall electric charge in each discharge cell depending upon information, and a display period for performing display of light emission, by means of the wall electric charge, are separated from each other, as the time periods being common with all the cells, to be driven. A ratio of the time period for light emission in the sub-field comes to be the length of this display period. In this manner, separation between the address period and the display period enables great simplification in the structure of a driver circuit.

High brightness display can be achieved by increasing of the number of driving pulses (sustain pulses), however there occurs a problem of increasing up electric power consumption therein. For realizing the high brightness display, but without the rise-up

of the number of those sustain pulses, there are necessities for, such as, increase of brightness of fluorescence substance, increase of the numerical aperture of cells, increase of ultraviolet light rays emitted from Xe atom with increasing pressure of the enclosed gas therein, etc. Those technologies for increasing the brightness also directly reaches to high efficiency of light emission.

Determining factor on the brightness in this plasma display device is the sum of the display period in each the sub-field within the one (1) field and/or also the numerical aperture of the cells of the panel itself. Hereinafter, explanation will be given on the structure of a panel of the conventional art relating thereto, by referring to Figs. 2 and 3, and then on a driving method of one (1) sub-field by referring to Fig. 4, and further on a reason of why the brightness cannot be increased up sufficiently with such the method.

Fig. 2 is an exploded perspective view of the structure of the above-mentioned panel. Upon a transparent surface plate 20 are formed a pair of transparent X electrode and Y electrode from ITO 201, on which are formed bus electrodes 202 having high conductivity. Those X and Y electrodes are formed alternatively on the surface plate, and further on them are formed a protection film 204 of MgO. On a while, on a substrate 205 are formed ribs 206 for defining the discharge cells therebetween, by means of a sand blast method, wherein on the bottom portions thereof are formed address electrodes 207 and fluorescent substances 208(R), 208(G) and 208(B) of three (3) colors, in a stripe-like shapes or manner. Those surface plate 200 and the substrate 205 are combined with each other and sealed hermetically, and then Ne-Xe mixture gas is filled up with in an inside thereof at pressure of 300-500 Torr.

Fig. 3 shows the structure of connection of electrode wirings and driver circuits of the panel. On the plasma display panel, each display lane is formed with the X electrode and the Y electrode

in a pair in the horizontal direction, and address electrodes A are disposed in the direction of crossing over them, wherein the discharge cells 101 are constructed at the intersection points of them. Those X electrodes are commonly connected to a sustain driver 105 for applying a rest pulse in each sub-field (which will be mentioned later) and a sustain pulse in a display period. On a while, to the Y electrodes are connected scan ICs 102, each applying a scanning pulse in the address period of each, and to each of the scan ICs is connected a sustain driver 104, thereby applying the sustain pulses to them in common in the display period. The address electrodes are connected to address ICs (not shown in the figure), to be applied with address pulses depending upon information, respectively.

Fig. 4 shows waveforms of driver voltages which are applied onto the X electrodes and the Y electrodes within the address period and the display period in one (1) sub-field. The address period is divided into two (2); i.e., the reset period for preparing address and the scanning period, wherein during this reset period, there is conducted the pilot light discharge, for the purpose of making ease and certain the erase operation of the wall electric charge, which is developed in the previous sub-field, and the write-in operation to be performed in the scanning period. A rest pulse 400 shown in the Fig. 4 is applied to all of the X electrodes (X1-X480) in common, thereby causing strong discharges on all the lines between the Y electrodes. When the reset pulse 400 falls down to 0V, self-erase discharge occurs between the X electrode and the Y electrode due to electric field developed as a result of the wall electric charge itself, thereby erasing all the wall electric charges caused by the reset discharges, and at the same time, residual spatial electric charges are remained in the discharge cells, so as to make them the pilot light for the write-in discharges in the next coming scanning period. In the scanning period, the scanning pulses 401 are applied to electrodes Y1, Y2...Y480 in that order, and line selection is conducted by that scanning pulse 401. To the address electrodes are applied address pulses 405

depending upon information, and the write-in discharge occurs between the electrodes A and Y when the scanning pulses 401 and the address pulse 405 coincide with each other in time. As a trigger of this write-in discharge operation, discharge occurs between the X electrode (to which the bias 404 is applied) and the Y electrode in each of those discharge cells, on which the write-in discharges are conducted, thereby developing the wall electric charge between the X and Y electrodes. The charge cell, in which the wall electric charge is developed, carries out the electric discharge for display upon receipt of the alternating sustain pulses 402 and 403 on the X and Y electrodes in the next display period, thereby performing the light emission for display. In the discharge cell, on which no address pulse 405 is applied to, since no write-in discharge will occur, nor the wall electric charge will developed, therefore the light emission for display will not performed even when the sustain pulse is applied thereto during the display period.

Next, explanation will be given on difficulty in rise-up of the brightness, in the example of the plasma display device. The electrode wiring of the panel mentioned above, which was listed up as the one example of the technologies relating thereto, is that in the case of XY/XT type, in which the X electrode and the Y electrode are disposed one by one. As shown in the Fig. 3, the lines of display are formed on the discharge cells 101 defined between the X electrode and the Y electrode in a pair, and there also exists a non-light emission area or region d. If the discharge occurs in this non-light emission region, it results into an operation error, therefore this non-light emission region must be wide sufficiently. This means that it decreases down the numerical aperture, i.e., a ratio of the light emitting portion on the panel, and this numerical aperture is about 30% in the conventional panel. With such the low numerical aperture, the panel falls down the light emission brightness thereof.

Also, in the driving methods, there are provided the address period and the display period in one (1) sub-field, and the display

period is determinative of the light emission brightness. However, in this address period, it is further provided into the reset period and the scanning period therein, and a time period of about 160 μs is necessary for it, so as to reduce the spatial charge sufficiently, during this reset period. Also, the time period from 1.5 μs to 2.0 μs is necessary, from the necessity of developing the wall electric charge within the write-in operation during the scanning period, with certainty, and in the case of 480 pieces in the line number thereof, the scanning period is needed to be equal or greater than 72 0μs. If the line number is equal or more than 1,000, for such as the HDTV, the address period for one (1) sub-field must be equal or more than 1.6ms. By the way, for reducing the pseudo-contour obstruction sufficiently with high gradation, for example, 256 steps of gradation, on the moving picture, the sub-fields are needed to be 10 to 12 in the number thereof, and in the case of achieving such the driving, all the times in the one (1) field (about 16.7 ms) is consumed only for the address period, but the display period can scarcely provided therein. Even if being possible to provide the display period, but it is impossible to ensure the brightness since it is less than 1 ms. If reducing the number of the sub-fields down to about 6, the display period can be provided for about 7 ms, however the gradation is decreased down to 64, therefore it is impossible to reduce the pseudo-contour obstruction.

With such the panel structure and such the driving method according to the conventional technology relating thereto, the gradation is less, when trying to perform the high definition display thereon, and also the improvement is insufficient against the pseudo-contour obstruction, therefore it is impossible to obtain sufficient brightness.

In such the related technologies, the high definition display of picture and the reduction of pseudo-contour obstruction are contrary to each other in directions thereof. Namely, the display line must be large in the number for realizing the high definition

display, and because of it, the time assigned to one (1) line is shortened. In more detail, for the drive of the plasma display panel, the scanning pulses are applied to, sequentially, so as to conduct the line selection, and causes the write-in (addressing) discharge in all the selected pixels depending upon information. For this reason, when the line number becomes large, the scanning pulses assigned for the line selection must be narrowed in pulse width thereof. However, a certain degree of time is necessary for occurring and settling of the address discharges, sufficiently on the AC type panel. For this reason, it is impossible to make narrower the pulse width of the scanning pulse, simply in inversely proportional to the increase of the line number. Therefore, it is commonly conducted that the scanning pulse is narrowed in the pulse width to a certain degree, while accompanying with this, the number of the sub-field is also decreased, so as to perform the display.

The decrease of the sub-fields in the number thereof results in, not only the decrease of the number in the gradation, but also the difficulty in reduction of the pseudo-contour. As an example of the measures for reduction in the pseudo-contour obstruction, there is a technology, in which a ratio of the width of display time period of the sub-field is encoded by the code other than the binary one, and in particular, wherein two (2) or more of the sub-fields are provided, being equal each other in the width of display time period, while making distinction or difference between lightening (actuation) and non-lightening (non-actuation) of those sub-fields for the pixel or the field, etc., thereby reducing the pseudo-contour appearing on the display screen. However in this case, the reduction of the number of the sub-fields results in, not only the difficulty in providing the sub-fields to be equal in the display time period, but also the decrease in the number of the gradation.

In the relating technology mentioned above, though tying to form the pixels at high density with smaller number of the

electrodes while utilizing the display areas effectively, for obtaining the high definition display, and cut off the total sub-field into a portion within the period thereof, or increasing the number of the sub-fields, for taking the measures against the pseudo-contour, however, no consideration was paid about the measures for protecting the display from the pseudo-contour appearing thereon, and measures against reduction of the address time period, etc., accompanying with such the high definition.

An object, according to the present invention, is to provide a new technology, with which a picture can be displayed with high gradation, being improved in the pseudo-contour, and at high brightness, as well as the high definition display thereof.

DISCLOSURE OF THE INVENTION

For achieving the above-mentioned object, according to the present invention, there are provided the following:

1) An display apparatus, for conducting video display through address operation on display lines upon basis of a video signal, wherein: scanning pulses of same phase are applied to plurality of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to plurality of second display lines in a second field thereof, thereby conducting the address operation.

2) An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein: scanning pulses of same phase are applied to the X electrodes of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to the Y electrode of second display lines in a second field thereof, thereby conducting the address operation, so as

to perform video display thereon.

3) An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein: scanning pulses of same phase are applied to plural numbers of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to plural numbers of second display lines, neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

4) An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein: said X and Y electrodes are disposed in reversed in the order thereof on display lines neighboring to each other; scanning pulses of same phase are applied to the X electrodes of plural number of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to the Y electrodes of plural numbers of second display lines, neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

5) An display apparatus, comprising parallel display electrodes X(i) (i = 1 through n (n: a positive number), an electrode of i^{th} number), and address electrodes A(j) (j = 1 through k (k: a positive number), an electrode of j^{th} number), being separated and crossing over said display electrodes X(i), wherein: conducting light emission display on the display electrodes X(4p+1) and X(4p+2) (p: a positive number including zero (0)), in a first period of a first field; conducting light emission display on the display

electrodes X(4p+3) and X(4p+4), in a second period of the first field; conducting light emission display on the display electrodes X(4p+2) and X(4p+4), in a third period of a second field; and conducting light emission display on the display electrodes X(4p+4) and X(4p+5), in a fourth period of the second field.

6) An display apparatus, comprising parallel display electrodes X(i) (i = 1 through n (n: a positive number), an electrode of i^{th} number), and address electrodes A(j) (j = 1 through k (k: a positive number), an electrode of j^{th} number), separately crossing over said display electrodes X(i), wherein: forming a pair with the display electrodes X(3p+1) and X(3p+2) (p: a positive number including zero (0)), and conducting light emission display on the display electrodes of said pair, in a first period of a field; forming a pair with the display electrodes X(3p+2) and X(3p+3) and conducting light emission display on the display electrodes of said pair, in a second period of the field; and forming a pair with the display electrodes X(3p+3) and X(3p+4) and conducting light emission display on the display electrodes of said pair, in a third period of the field.

7) A display apparatus, constructing a display screen by disposing discharge cells in a matrix-like manner, each discharge cell being constructed with a pair of display electrodes being parallel to each other and covered with a dielectric body, and with a set of an address electrode being disposed in a direction of crossing thereover, wherein: address electrodes are disposed in common for a first panel portion and a second panel portion, constructing said display screen therewith; operating address operation, sequentially, all said discharge cells of said first panel portion, by scanning one of the pair of display electrodes of said first panel portion, sequentially, while applying a selection pulse between the display electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said first panel portion of said discharge cells being operated by the address operation,

simultaneously, thereby conducting display sustain operation; and operating address operation, sequentially, all said discharge cells of said second panel portion, by scanning one of the pair of display electrodes of said second panel portion, sequentially, while applying a selection pulse between the display electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said second panel portion of said discharge cells being operated by the address operation, simultaneously, thereby conducting display sustain operation; and further having: a time band, during which the address operation of said first panel portion and the display sustain operation of said second panel portion coincide with each other.

8) A display apparatus, having at least plural numbers of parallel scan electrodes and plural numbers of parallel address electrodes crossing over said scan electrodes separately, wherein discharge cells are formed at intersection points of said scanning electrodes and said address electrodes, and said discharge cells are disposed in a matrix-like manner, wherein: applying scanning pulse to said scanning electrode for conducting line selection, applying address pulse depending upon information onto said address electrode, and applying voltage for sustaining said address discharge after completion of application of said scanning pulse, onto the scan electrode just after completion of said scanning pulse, in the address operation for conducting write-in by causing the address discharge which is caused by said scanning pulse and said address pulse.

9) A display technology, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing a display line and an address electrodes which crosses over said display electrodes, wherein: an address electrode is provided being connected in common to a first panel portion and a second panel portion, and an address period of a sub-field in said first panel portion and a display period of a sub-field in said second panel portion overlap with

each other.

19) A video display apparatus, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing first and second display lines and an address electrodes which crosses over said display electrodes, comprising: means for conducting same address operation by applying scanning pulses of same phase to said first display line of plural number of display lines, and a driver portion for driving plural numbers of display electrodes with driving pulses differing from each other.

With such the structure, according to the present invention, it is possible to reduce the scanning time in address period and the pseudo-contour obstruction with high gradation, since it enables a driving of a large number of sub-fields, and also to realize a display technology with high brightness. With the structure of the above 4), since a panel can be realized with high numeral aperture, it has high brightness, and also because of the sameness in address discharge conditions between the first field and the second field, write-in operation can be conducted with stability. Also, it is possible to reduce cross talk between address discharges. Further, in this case, since it is possible to use a same scanning electrode as an electrode for use of scanning between the the first field and the second field, it is possible to obtain compatibility between the progressive display for the display of personal computer. Also, differentiating voltage values of the address pulses to be applied between the first field and the second field enables a driving with address pulses fitting with characteristics of address discharges in the first field and the second field, thereby realizing a stable operation. Also, with the structure of the above 5), it is possible to drive the neighboring display lines by every fourth line thereof, i.e., a four (4) phases, on all of the parallel electrodes X up and down, therefore the display can be conducted in a time of about a half (1/2) of one (1) field in each one of the phases. With this, both high definition

and reduction of the pseudo-contour obstruction can be realized. With the structure of the above 6), since it is possible to divide one (1) field into three (3) periods with three (3) phase drive for each three (3) lines, thereby to perform display in each period and in each phase, the display period of a one (1) line can be cut off in time down to about one-third (1/3) of the (1) field. With the structure of the above 7), display sustain operation is conducted in the second panel portion while operating address operation in the first panel portion, the utilization factor of time is high, and then much large number of sustain pulses can be applied to, therefore the high brightness can be obtained. Also, with the structure, in which address electrodes are wired in common on both sides of the panel, it is possible to reduce the number of address electrode driver circuits, as well as, the cost thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the structure of a driver circuit, which is applied into an apparatus, according to the present invention;

Fig. 2 shows an exploded perspective view of a plasma panel, as the conventional technology relating thereto;

Fig. 3 shows the structure of a driver circuit for a panel of XY/XY type, as the conventional technology relating thereto;

Fig. 4 shows waveforms of driver voltages for the panel, as the conventional technology relating thereto;

Fig. 5 shows waveforms of driver voltages of driver circuits, which are applied into the apparatus according to the present invention;

Fig. 6 shows a display method by means of the apparatus according to the present invention;

Figs. 7(a) and 7(b) are views for explaining numerical aperture of a panel;

Fig. 8 shows waveforms of driver voltages of driver circuits which are used in the apparatus according to the present invention;

Fig. 9 shows the structure of the driver circuits which are used in the apparatus according to the present invention;

Fig. 10 also shows the structure of the driver circuits which are used in the apparatus according to the present invention;

Fig. 11 shows other waveforms of driver voltages of driver circuits which are used in the apparatus according to the present invention;

Fig. 12 shows a display method of display cells (a line) of the panel in the apparatus according to the present invention;

Fig. 13 shows the structure of sub-field in the apparatus according to the present invention;

Fig. 14 shows waveforms of driver voltages of driver circuits which are used in the apparatus according to the present invention;

Fig. 15 shows the structure of the apparatus according to the present invention;

Fig. 16 shows other structure of the apparatus according to the present invention;

Fig. 17 shows other waveforms of driver voltages according to the present invention;

Fig. 18 shows other structure of the sub-fields in the apparatus according to the present invention;

Fig. 19 shows further other structure of the sub-fields in the apparatus according to the present invention;

Fig. 20 shows a display method of display cells (a line) of the panel in the apparatus according to the present invention;

Fig. 21 shows the other structure of sub-field in the apparatus according to the present invention;

Fig. 22 shows other waveforms of driver voltages which are used in the apparatus according to the present invention;

Fig. 23 shows the structure of driver circuits which are used in the apparatus according to the present invention;

Fig. 24 shows a driving method of the apparatus according to the present invention;

Fig. 25 shows a scanning method in an upper portion of the panel, which is used in the apparatus according to the present invention;

Fig. 26 shows a scanning method in a lower portion of the panel, which is used in the apparatus according to the present invention;

Fig. 27 shows the structure of the panel with horizontal ribs in the apparatus according to the present invention;

Fig. 28 shows a driving method of the panel with horizontal ribs, according to the present invention;

Figs. 29(a) and 29(b) show a relationship between a display sustain pulse and an address pulse in the apparatus according to the present invention;

Fig. 30 shows an scanning pulse and discharging condition in the apparatus according to the present invention;

Fig. 31 shows the scanning pulse and the discharging condition in the conventional apparatus according to the prior art;

Fig. 32 shows voltage waveforms applied to respective electrodes in the apparatus according to the present invention; and

Fig. 33 shows other voltage waveforms during an addressing period in the apparatus according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

For better understanding thereof, the present invention will be explained in more details hereinafter.

First embodiment of the present invention will be explained by referring to Figs. 5 and 6.

Fig. 6 is a view for explaining a display method by means of an apparatus according to the present invention. As television signals, on a first field, video signals of 1st line, 3rd line, 5th line...are transmitted, however displays of those signals are so that the same one is displayed on two (2) lines of the following sets, (1,2), (3,4), (5,6)..., for example. On a second field, video signals are transmitted on 2nd line, 4th line, 6th line..., however displays of those signals are so that the same one is displayed on two (2) lines of the following sets, (2,3), (4,5), (6,7). In this manner, the same display on two (2) lines is carried out with shifting them on the first field and the second field by one (1) line. Now, in the case of the high definition video signal having display lines of such the HDTV, the number of display lines comes up to 1,000 lines or more. When conducting the same display on two (2) lines for such the high definition video or picture,

resolution in the vertical direction is lowered down. As a criterion indicative of the decrease in the resolution is known by the Kell coefficient, and if setting this Kell coefficient at 0.7, for example, the resolution thereof comes down to around 700 lines. However, the decrease of this resolution is same to a CRT (Cathode Ray Tube), and it scarcely causes a problem in the display on the television apparatus.

Fig. 5 shows waveforms of driver voltages when the present invention is applied into the XY/XY panel of the related technology (see the Fig. 3). Herein is shown an address period (including a reset period and a scanning period) of the first sub-field. An aspect differing from the driver waveforms of the conventional technology relating thereto lies that scanning pulses of the same phase are applied onto two (2) scanning electrodes. On the XY/XY panel shown in the Fig. 3, as the display lines, 1st line, 2nd line, 3rd line...are constructed with the sets of electrodes, (X1,Y1), (X2,Y2), (X3,Y3)..., while scanning pulses are applied onto the Y electrodes, in a form of the scanning electrodes. As shown in this Fig. 5, in the first field, the scanning pulses 401 in the same phase are applied to Y1 and Y2 electrodes. With this application of those scanning pulses at the same phase, write-in operation by means of the address pulses on the address electrodes are same for both the Y1 and Y2 electrodes, therefore the same wall electric charges are developed on the 1st and 2nd lines. In the same manner, applying the scanning pulses of the same phase onto Y3 and Y4...develops the same wall electric charge on the 3rd and 4th lines. In a display period following after the scanning period, alternating sustain pulses 402 and 403 are applied onto the X and Y electrodes, however since the 1st and 2nd lines are same in the wall electric charges developed in the scanning period, light emissions thereof are also same on the 1st and 2nd lines during the display period. On the second field, as indicated by the reference numerals shown in parentheses of the Y electrodes, the scanning pulses of the same phases are applied onto Y2 and Y3 electrodes, Y4 and Y5 electrodes,..., thereby developing the same

wall electric charges thereon, and in the display period, the 2nd and 3rd lines and the 4th and 5th lines emit light, thereby performing display operation.

In this manner, with application of the scanning pulses of the same phase onto the Y electrodes of the two (2) lines, the same display is performed on the 2 lines, and then next display is conducted with shifting by one line, by changing the combination of lines of the scanning pulses to be applied at the same phase, between the first field and the second field.

In this manner, conducting the same display on 2 lines at the same time makes the scanning period one half (1/2) of the conventional one in the period. For example, in the case of the HDTV signal having 1,000 lines, assuming that width of the scanning pulse of one sub-field is 1.5 μs, the scanning period is 1.5 μs $\times$500=0.75 ms, and this is one half in the case of the progressive scanning (i.e., line sequential scanning).

With the time period that can be used for display in this case, a reset period is set at 160 μs for one (1) sub-field, and then it can be taken to be equal or more than 5.7 ms as the display period in one (1) field, even if conducting the display of 12 sub-fields, in which sufficient measures can be taken against the pseudo-contour with high gradation, therefore the display is possible with high brightness. Also, because of the same displays on two (2) lines, all of discharge cells are displayed during the period of one (1) field, and this is also a factor of enabling the display of high brightness.

Next, explanation will be given on a second embodiment, by referring to Figs. 1, 7 and 8.

The Fig. 3 shows a circuit diagram of electrodes of the XY/XY type panel, as the related conventional technology, wherein the X electrodes and the Y electrodes are disposed one by one. Disposing

condition of said electrodes are shown in Fig. 7 (a). The X electrode 700 and the Y electrode 701 build up the display lines in a pair thereof. Non-light emission region 300 must be provided to be sufficiently wide so that no error discharge occurs between the Y electrode and the X electrode. This means that the size 702 of the discharge cells is made small, and lowers the numerical aperture thereof.

On the contrary to this, two (2) pieces of the Y electrodes 705 are disposed between the X electrodes 704 on the XY/YX panel shown in the Fig. 7(b), and the electrodes neighboring with the non-display area 300 are the Y electrodes, or X electrodes, by themselves. For this reason, the sustain pulses for the neighboring two (2) electrodes are same in the phases thereof, then no discharge occurs between them. For this, the non-display region 300 can be formed narrowly while the display region 706 widely. Accordingly, with this panel, the numerical aperture can be made large, thereby to rise up the brightness in light emission.

The structure of a driver circuit is shown in Fig. 1, in the case of conducting the same display on two (2) lines with using that XY/YX type panel, and waveforms of the driver voltages thereof in Fig. 8. A plasma display panel 100 in the Fig. 1 has wiring of the XY/YX type, and forms discharge cells at intersection points of the X electrode, the Y electrode and the address electrode. Between the neighboring two (2) pieces of Y electrodes, and between the neighboring two (2) pieces of X electrodes, there are defined non-light emission regions 106, wherein light shielding members are provided, so as to heighten contrast under a bright room. The neighboring Y electrodes (i.e., Y1 and Y2, Y3 and Y4,...) are connected by themselves in common, to be connected with scan ICs 102, for outputting scanning pulses therefrom, and those scan ICs 102 are connected in common with a sustain driver 104 for generating a sustain pulse therefrom. On a while, the neighboring X electrodes (i.e., X2 and X3, X4 and X5,...) are connected by themselves in common, to be connected with scan ICs 103, for outputting scanning

pulses therefrom, and those scan ICs 103 are connected in common with a sustain driver 105 for generating a sustain pulse therefrom.

Fig. 8 shows voltage waveforms on one (1) sub-field, which are applied to the X electrodes and the Y electrodes in the structure shown in the Fig. 1. In the first field, the scanning pulse is applied onto the Y electrode, so as to make it as the scanning electrode, and in the second field the scanning pulse is applied onto the X electrode, so as to make it as the scanning electrode. In the first field, a reset pulse 400, a bias pulse 404 and a sustain pulse 402 are applied in common onto all of the X electrodes (X1-X1024). The Y electrodes, Y1 and Y2, Y3 and Y4,...are connected in common, and the scanning pulses 401 are applied to those electrodes, one by one. Since Y1 and Y2, Y3 and Y4,...are connected in common, the same display is made on the display lines in a pair, such as, 1 and 2, 3 and 4,... While on the second field, the reset pulse 400, the bias pulse 404 and the sustain pulse 402 are applied in common onto all of the Y electrodes (Y1-Y1024). The X electrodes, X1 and X2, X3 and X4,...are connected in common, and the scanning pulses 401 are applied to those electrodes, one by one. Since X1 and X2, X3 and X4,...are connected in common, the same display is made on the display lines in a pair, such as, 2 and 3, 4 and 5,... Accordingly, the same display is made on two (2) lines in the first field and the second field. With adopting such the driving method of wiring of the X and Y electrodes, two (2) pieces of the electrodes, onto which the scanning pulses of the same phase are applied in the first field and the second field, are always neighboring with each other. Accordingly, since the conditions are same in the address discharges between the first field and the second field, a stable discharge characteristics can be obtained.

Next, explanation will be given on a third embodiment by referring to Fig. 9. Though the wiring of X and Y electrodes on a panel 100 is the XY/YX type, being same in the case of the Fig. 1, however it differs from the case of the Fig. 1, in the condition

that two (2) pieces of the scanning electrodes are connected in common so as to display the same on two (2) lines. In the structure of the Fig. 9, the Y electrodes are connected in common, such as , Y2 and Y3, Y4 and Y5,..., and are connected to the scan ICs 102, each outputting the scanning pulse, and the sustain driver 104. On the other hand, the X electrodes are connected in common in a pair, such as, X1 and X2, X3 and X4,..., and are connected to the scan ICs 103, each outputting the scanning pulse, and the sustain driver 105. In the first field, the scanning pulses are applied to the X electrodes, sequentially, as the scan electrodes, thereby displaying the same onto 2nd and 3rd, 4th and 5th,...of the display lines. An aspect differing from the Fig. 1 lies that the scanning electrodes do not always neighbor between the first and second fields, onto which the scanning pulses of the same phase are applied, and that other two (2) display electrodes are inserted therebetween. With the structure of this Fig. 9, since the address discharges are same in the condition between the first field and the second field, the operation is stable, and further since the discharge cells applied with the scanning pulses of the same phase are not neighboring with each other, stroke in the address discharge can be reduced.

Next, explanation will be given on a forth embodiment, by referring to Figs. 10 and 11. In the Fig. 10, the panel 100 has the wiring of electrodes of the XY/YX type, same to the case of the Fig. 1, however the Y electrodes are connected to the scan ICs 102, respectively, and the sustain driver 104 is connected to said the scan ICs. All the X electrodes are connected to the sustain driver 105, in common.

Fig. 11 shows waveforms of driving voltage on the X and Y electrodes. In the first field, a reset pulse 400, a bias pulse 404 and sustain pulses 402 are applied onto all of the X electrodes (X1-X1024) in common. To the Y electrodes, scanning pulses 401 of the same phase are applied, one by one, such as, Y1 and Y2, Y3 and Y4,... With this, the same is displayed on 1st and 2nd lines,

3rd and 4th lines of the display lines. In the second field, the reset pulse 400, the bias pulse 404 and the sustain pulses 402 are applied onto all of the X electrodes. To the Y electrodes, scanning pulses 401 of the same phase are applied, one by one, such as, Y2 and Y3, Y4 and Y5,... In this manner, as a method for outputting the scanning pulses of the same phase by means of each scan IC, there is a way, in which control is conducted in a signal processor portion, such as, a shift register installed within the scan IC, so as to output the scanning pulses of the same phase, and also other way, in which the ICs in an order of odd number and in an order of even number are divided in a form of the separated ICs (generally, there are 64 outputs on one IC). In this case, electrical connection from the scan ICs to the panel may be constructed with a FPC (Flexible Print Circuit) of two (2) layers, etc. In the case where such the Y electrodes are fixed as the scanning electrodes while applying the scanning pulses of the same phase through the respective scan ICs, two (2) pieces of the Y electrodes, onto which the scanning pulses of the same phase are applied, are neighboring to each other in the first field, but the two (2) pieces of the Y electrodes, onto which the scanning pulses of the same phase are applied, are not, in the second field. In the case where the driving conditions differ between the first field and the second field in this manner, it is possible to obtain stable address discharge operations by changing the voltage values of the address pulses in the first field and the second field. When the scanning pulses of the same phase are applied to the electrodes of the first fields neighboring with each other, since the starting voltage of discharge is low, voltage Va1 of a low pulse address pulse is applied to, as indicated by a reference numeral 1100 in the Fig. 11, while when applying the scanning pulses of the same phase to the electrodes of the second field not neighboring with each other, since the starting voltage of discharge is high, voltage Va2 of a high pulse address pulse is applied to, as indicated by a reference numeral 1101 in the Fig. 11.

Also, since application of the scanning pulses is fixed onto

the Y electrodes in this manner, and since the scan ICs are connected to the Y electrodes, respectively, the progressive scanning is possible by changing over the display between the television apparatus and the personal computer, and also the flicker-less display of the personal computer without the interlace display, as well.

Next, explanation will be given on a fifth embodiment, by referring to Figs. 12 through 15. Herein, all display electrodes of the plasma display are X electrodes, and they are attached with a sequential number in the order thereof from the above.

Fig. 12 shows a method for forming a pair of the display electrodes X according to the present invention, and a display method thereof. With the structure of the Fig. 12, there is shown an example, where thirteen (13) pieces of the display electrodes X and five (5) pieces of the address electrodes are used. First of all, the first frame (1/30 sec.) is divided into the first and second fields (each, 1/60 sec.), and further the first field is divided into first and second periods while the second one into third and fourth periods. In this case, if the first and second periods and the third and fourth periods are equal to one another, then it comes to be 1/120 sec each.

In the first period of the first field, the X electrodes form the display lines in a pair thereof, i.e., X(1)-X(2), X(5)-X(6), X(9)-X(10), respectively, and form display cells at the intersection points with the address electrodes. On a panel having a large number of the display electrodes thereon, the electrodes, X(4p+1)-X(4p+2) (where, "p" is a positive number including zero (0)), form the display lines in a pair thereof. The address discharge is initiated by applying the scanning pulse onto one of the pair of the display electrodes X. During the display period, onto those two (2) pieces of the display electrodes X of this pair are applied sustain pulses, which are reversed to be opposite to each other in polarity thereof, thereby causing the display charge (i.e.,

sustain discharge). Neither the scanning pulse nor the sustain pulse is applied to the electrodes, X(3), X(4), X(7), X(8), X(11), X(12), but DC voltage is applied thereto, so as to prevent error discharge from occurring between those neighboring electrode.

In the second period of the first field, the X electrodes form the display lines in a pair thereof, i.e., X(3)-X(4), X(7)-X(8), X(11)-X(12), respectively, and form display cells at the intersection points with the address electrodes. On a panel having a large number of the display electrodes thereon, the electrodes, X(4p+3)-X(4p+4) (where, "p" is a positive number including zero (0)), form the display lines in a pair thereof. This display line is located just at the middle on the display line, which is formed in the first period of the first field. Namely, it is the display in which the first period and the second period are interlaced with each other in the first field.

In the third period of the second field, the X electrodes form the display lines in a pair thereof, i.e., X(2)-X(3), X(6)-X(7), X(10)-X(11), respectively, and form display cells at the intersection points with the address electrodes. On a panel having a large number of the display electrodes thereon, the electrodes, X(4p+2)-X(4p+3) (where, "p" is a positive number including zero (0)), form the display lines in a pair thereof.

In the fourth period of the second field, the X electrodes form the display line in a pair thereof, i.e., X(4)-X(5), X(8)-X(9), X(12)-X(13), respectively, and form display cells at the intersection points with the address electrodes. On a panel having a large number of the display electrodes thereon, the electrodes, X(4p+4)-X(4p+5) (where, "p" is a positive number including zero (0)), form the display lines in a pair thereof. This display line is located just at the middle on the display line, which is formed in the first period of the second field, thus, obtaining the interlace display between the third and fourth periods in the second field.

In this manner, for example like the display electrode X(2), by taking into the consideration the facts that it is one of the electrodes forming the display line in the first period of the first field and the third period of the second field, and further that the display line is shifted at both ends thereof and that the display electrode of X(2) forms the display lines with the display electrodes of X(1) and X(3) in a pair, in total, a ratio comes to be the same in the case where one (1) display line is formed with one (1) piece of the display electrodes X, therefore the video display of high definition can be achieved.

As is shown below in the Fig. 12, assuming that the display line formed in the first period of the first field is a display line of 1st phase, the display line formed in the second period of the first field a display line of 2nd phase, the display line formed in the third period of the second field a display line of 3rd phase, the display line formed in the fourth period of the second field a display line of 4th phase, respectively, then the interlace display can be obtained on those of the 1st and 2nd phases, and 3rd and 4th phases, as well, and further the interlace display can be also obtained between an addition of the 1st and 2nd phases of the first field and an addition of the 3rd and 4th phases of the second field. Accordingly, repetition of the displays seemingly rises up in the number thereof, and the phenomenon of flicker can be suppressed, thereby improving quality of the picture.

Fig. 13 shows a display method in the apparatus according to the present invention, in particular, a method for forming the sub-fields of four (4) phases. Herein, though there is shown an example, in a case where the sub-fields are three (3), but in a case of obtaining color display, the sub-fields are provided in the number of eight (8) or more.

In a set of the electrodes X(4p+1)-X(4p+2) on the 1st phase display line, all the sub-fields are provided within the first period of the first field. With the sub-fields, a case of three

(3) sub-fields SF1, SF2, and SF3 is shown in the figure, wherein each sub-field is divided into an address period (A1,A2, A3) and a display period (S1,S2, S3). In the address period, the scanning pulse is applied onto one of the display electrodes X in a pair, and onto the address electrode is applied an address pulse depending upon information, wherein the scanning pulse and the address pulse initiates address discharge in a display cell where they coincide with in timing, so as to develop the wall electric charge therein. In the display period, the sustain pulses changing over alternatively in polarity are applied onto the display electrodes in a pair, and then only the cell in which the wall electric charge is developed during the address period occurs discharge upon the sustain pulse, thereby achieving the display operation. Herein, the number of the sustain pulses differs in each of the sub-fields. For example, assuming that the number of the sustain pulses SF1, SF2 and SF3 is 1:2:4, it is possible to obtain the display in eight (8) steps of the gradation with the combination thereof.

Also, in a pair of the electrodes X(4p+3)-X(4p+4) on the 2nd phase display line, all the sub-fields are provides within the second period of the first field, in a pair of the electrodes X(4p+2)-X(4p+3) on the 3rd phase display line, all the sub-fields are provides within the third period of the second field, and in a pair of the electrodes X(4p+4)-X(4p+5) on the 4th phase display line, all the sub-fields are provides within the fourth period of the second field, respectively.

In this manner, all the sub-fields of each phase are within a time period of about a half (1/2) of one (1) field, therefore it is possible to reduce the pseudo-contour greatly when displaying the moving picture. Also, in a case of trying to apply the display technology according to the present invention into the display of television signal, signals on the 1st and 2nd phases are displayed with the video signals transferred in the first field. In this case, since there is time difference of about 1/2 field in the display timing between the 1st phase and the 2nd phase, the video

signal on the 2nd phase may be corrected one, which is compensated in the movement thereof. Also, the signals on the 3rd and 4th phases are displayed with the video signals transferred during the second field. This causes no shift on the picture when being displayed as it is, without movement compensation thereon, since the combination of the 1st and 2nd phases and that of the 3rd and 4th phases are interlaced with each other in the display, and since the television signal is also interlaced between the first field and the second field thereof. Also, when the display signal of the 4th phase is the corrected signal which is compensated in the movement, the quality of display can be improved.

Fig. 14 shows waveforms of voltages to be applied to each of the electrodes, in the display of the 1st phase during the first period of the first field. Herein, only a case of SF1 is shown.

Onto each of the display electrodes X(1), X(5), ..., X(4p+1)... is applied voltage VX1, including a full write-in pulse 400 and sustain pulses 402.

Onto each of the display electrodes X(2), X(6), ..., X(4p+2)... is applied voltage VX2, in which a scanning pulse 401 is superimposed on a bias 403 and includes sustain pulses 402. Herein, the scanning pulses 401 are applied onto the display electrodes, sequentially, with shifting in timing, in the order of X(2), X(6), X(10)...

Onto each of the display electrodes X(3), X(7), ..., X(4p+3)... is applied voltage VX3, including DC voltage 1406 for preventing error discharge from occurring upon the sustain pulse on the neighboring display electrode, such as, the display electrode X(2). A value of this DC voltage is set to be the voltage value lower than that of the sustain pulse, and preferably to be about a half (1/2) of the voltage value of the sustain pulse.

Onto each of the display electrodes X(4), X(8), ..., X(4p+4)... is applied voltage VX4, including the full write-in prevention

pulse 1407 for preventing error discharge from occurring between the full write-in pulse on the neighboring display electrode, such as, the display electrode X(5), and DC voltage 1408 for preventing error discharge from occurring upon the sustain pulse. A value of this write-in prevention pulse is set to be the value, obtained by subtracting the starting voltage of discharge from the full write-in pulse 400, or more than that.

On a while, onto the address electrode is applied voltage of VA, including a full write-in prevention pulse 1409, an address pulse 405 depending upon information, and a sustain pulse discharge prevention DC voltage 1411. Herein, the address period A1 of the sub-field shown in the Fig. 13 is such that, including the full write-in pulse and the scanning pulse 401 therein, and the display period S1 is such that, including the sustain pulse therein.

Next, discharge condition will be explained by referring to Fig. 14.

When the full write-in pulse 400 is applied onto the display electrode X(4p+1), discharge occurs between the neighboring display electrode X(4p+2). Herein, though there lies also the electrode X(4p) neighboring thereto, however no discharge occurs since the full write-in prevention pulse 1407 is applied thereto. Also, since the full write-in prevention pulse 1407 is applied to the address electrode, no discharge occurs between this electrode. This full write-in pulse has also a function of resetting information of the wall electric charge, which is written into the sub-field in advance by one.

Next, when the voltage value of the full write-in pulse 400 comes down, since the wall electric charge caused in the full writer-in charge is much enough (the voltage value of the full write-in pulse is sufficiently large), self-erase discharge (full-erase discharge) occurs. The full-erase discharge is discharge, in which the wall electric charge is floated into space

within the cell, so as to neutralize ion and electron, thereby erasing the wall electronic charge caused in the full write-in discharge.

Next, the scanning pulse is applied onto the display electrode X(4p+2), and then address discharge occurs between the address pulse 405 on the address electrode, and making this address discharge as a trigger, the discharge occurs between the display electrode X(4p+1) and the display electrode X(4p+2). With this discharge, electron is developed in a form of electric charge on the electrode X(4p+1) while ion on the electrode X(4p+2). Next, in the display period, first of all when the first one of the sustain pulses 403 is applied onto the display electrode X(4p+2), voltage of the wall electric charge of ion and that of the sustain pulse are superimposed with each other, thereby causing the discharge. Thereafter, with applying the sustain pulses onto the display electrodes X(4p+1) and X(4p+2), alternatively, the voltage superimposed with that of the wall electric charge exceeds the starting voltage of discharge, and the discharge is succeeded. The electrodes other than the display electrodes X(4p+1) and X(4p+2) are applied with sustain pulse discharge prevention DC voltage, and further no wall electric charge is developed on those electrodes, therefore no discharge occurs.

In the above, description was given on the driving waveforms of the SF1 in the first period of the first field, however those of the SF2 and SF3 are also same to the cases shown in the Fig. 14, but only differ from them in the number of the sustain pulses in the sub-field.

Next, assignment is shown in a Table 1, of voltages, being applied to the respective electrodes during the 1^{st}, 2^{nd}, 3^{rd} and 4^{th} periods of the first and second fields. With assignment of voltages to be applied to the respective display electrodes X in this manner, only the display electrodes X of even numbers are applied with the scanning pulses, and as a result of this, the

circuit comes to be simple in the construction thereof.

Table 1

	First Field		Second Field	
	1st Period	2nd Period	3rd Period	4th Period
X(1)	VX1	VX3	VX3	VX1
X(2)	VX2	VX4	VX2	VX4
X(3)	VX3	VX1	VX1	VX3
X(4)	VX4	VX2	VX4	VX2
X(5)	VX1	VX3	VX3	VX1
X(6)	VX2	VX4	VX2	VX4
X(7)	VX3	VX1	VX1	VX3
X(8)	VX4	VX2	VX4	VX2
X(9)	VX1	VX3	VX3	VX1
X(10)	VX2	VX4	VX2	VX4
X(11)	VX3	VX1	VX1	VX3
X(12)	VX4	VX2	VX4	VX2
X(13)	VX1	VX3	VX3	VX1

Next, the circuit structure will be explained on the plasma display panel display apparatus, according to the present invention, by referring to Fig. 15. This plasma display panel 100 is a panel of AC type. According to the Table 1, the scanning pulse and the sustain pulse are applied on the display electrodes of odd numbers while the full write-in pulse and the sustain pulse on those of even numbers, therefore the circuits to connected with differ between the display electrodes X of the even numbers and the odd numbers. Terminal portions of the address electrodes are drawn from the panel 100 onto upper and lower sides thereof, in the figure.

Next, explanation will be given by following flows of the signals shown in the Fig. 15. A video signal 1500 of analogue signal is converted into a digital video signal through an A/D converter 1501. This digital video signal is encoded into a binary code of a brightness level, and this is converted through a Bit-SF converter

(bit/sub-field converter) 1502 into a signal fitted to a code obtained by weighting of the display period of the sub-field. Herein, if the weighting of the sub-field is the binary code as it is, an output signal of the A/D converter is used as it is, i.e., as a signal of SF. However, the video signal 1500 is the television signal, an inverse compensation of γ (not shown in the figure) must be conducted here. The video signals fitting to the sub-fields are once stored into a field memory 1503, and then they are read out with the timing fitting to the address period of the each sub-field, wherein those are applied onto address electrodes of the panel 100 in the form of the address pulses of high voltage signals, which are necessary in address drivers A1506 and B1507.

On a while, the signals, such as, the full write-in pulse, the scanning pulse, the sustain pulse and the DC voltage, etc., are applied onto the display electrodes X irrespective of the video signal, and those signals are generated by a control signal generator circuit 1505. In the structure of this control signal generator circuit 1505, in more details, information is written into a ROM in advance, and is read out with the timing determined by clk (clock signal), H (horizontal synchronism signal), V (vertical synchronism signal), etc. Among outputs of this control signal generator circuit 1505, those including the scanning pulse are inputted into a scan-sustain driver A1510, so as to be converted into the scanning pulse and a high voltage signal, such as, the sustain pulse, and they are applied onto the X(4p+2) of the display electrodes X. To those electrodes, they are applied during the first period of the first field and during the third period of the second field, in accordance with the Table 1. Also, upon an output of the control signal generator circuit 1505, other signals, including the scanning pulse therein, are inputted into a scan-sustain driver B1511, so as to be converted into the scanning pulse and a high voltage signal, such as, the sustain pulse, and they are applied onto the X(4p+4) of the display electrodes X. To these electrode, they are applied during the second period of the first field and during the fourth period of the second field.

Also, those, including the full write-in pulse signal and the sustain pulse signal therein, are inputted from the control signal generator circuit 1505 into a sustain driver A1508, so as to be converted into a necessary high voltage pulse, and it is applied onto the X(4p+1) of the display electrodes X, in common. To those electrodes, it is applied during the first period of the first field and during the fourth period of the second field. Also, other signals, including the full write-in pulse signal and the sustain pulse signal therein, are inputted into a sustain driver B1509, so as to be converted into a necessary high voltage pulse, and it is applied onto the X(4p+3) of the display electrodes X, in common. To those electrodes, it is applied during the second period of the first field and during the third period of the second field. Also, to the X(4p+1) of the display electrodes X is applied the DC voltage, during the second period of the first field and during the third period of the second field, through the sustain driver A1508, in the display period. Also, to the X(4p+3) of the display electrodes X is applied the DC voltage, during the first period of the first field and during the fourth period of the second field, through the sustain driver B1509, in the display period. Also, to the X(4p+2) of the display electrodes X is applied the DC voltage of the full write-in discharge prevention pulse and the sustain pulse discharge prevention pulse, through the scan-sustain driver A1510, during the second period of the first field and during the fourth period of the second field. And also, to the X(4p+4) of the display electrodes X is applied the DC voltage of the full write-in discharge prevention pulse and the sustain pulse discharge prevention pulse, through the scan-sustain driver B1511, during the second period of the first field and during the third period of the second field.

Also, to all the address electrodes is applied the DC voltage of the full write-in discharge prevention pulse and the sustain pulse discharge prevention pulse, through the scan-sustain driver B1511.

Also, to all the address electrodes is applied the DC voltage of the full write-in discharge prevention pulse and the sustain pulse discharge prevention pulse, through the address drivers A1506 and B1507.

Next, explanation will be given on a sixth embodiment of the present invention, by referring to Figs. 16 and 17. An aspect differing from the fifth embodiment mentioned above lies in that two (2) of the display electrodes, onto which the scanning pulses are applied, are connected in common through connection of the panel electrodes, thereby enabling to cut the number of circuits outputting the scanning pulses down to a half (1/2).

Fig. 16 is a view of shows wiring of the electrodes on the panel. The display electrodes, onto which the scanning pulses are applied, are indicated by Y1, Y2, Y3..., while the other display electrodes by X1, X2, X3... Those Y and X electrodes are disposed one by one, alternatively. The X display electrodes forming a pair with the display electrode of Y1 are the display electrodes X1 and X3, neighboring with the Y electrode up and down or on both sides, and those electrodes forming the pair differ in timing of display, therefore the display never be conducted on both at the same time. Those relationships are same to the Y2, Y3..., too. Herein, Y1 and Y2, Y3 and Y4,..., in a pair are connected to the scan ICs (i.e., the integrated circuits for generating the scanning pulses), in common, and further, they are connected to Y collector circuits 1 and 2, functioning as the sustain pulse generators, alternatively by every second (2^{nd}) of the pair of Y electrodes (i.e., the scan ICs are connected to the Y collector circuits 1 or 2, by every second (2^{nd}) thereof), as shown in the same figure. On a while, the X electrodes are connected to X collector circuits 1, 2, 3 and 4, functioning as the sustain pulse generator circuits, respectively by every fourth (4^{th}) piece thereof. With such the connection condition of the display electrodes, since the X electrodes, X1, X2 and X3, forming pairs with the electrodes Y1 and Y2 up and down and being connected in common, are all connected

to the different circuits, respectively, therefore the X electrodes forming the pairs can be selected through controlling the output waveforms of the different X collector circuits, if the scanning pulse is applied onto the electrodes Y1 and Y2. Those relationships are same to the electrodes Y3 and Y4, and Y5 and Y6,..., too.

Fig. 17 shows the waveforms of driver voltages for driving, in the connection condition of the display electrodes of the panel shown in the Fig. 16. Herein, the waveforms shown are of the driver voltage on the electrodes from X1 to X5 and the electrodes from Y1 to Y5, and they are the voltage waveforms in one (1) sub-field under the condition that L1, L5 and L9 are selected by the display liens from L1 to L9. Thus, it shows the driving condition in one (1) sub-field within the first period of the first field shown in the Fig. 13. Herein, a driving method of address erase type is shown, as an example.

First of all, on a selection electrode of L1 at the 1st line, a reset pulse 1700 and sustain pulses 1703 are applied onto the electrode X1 from the X collector circuit 1. To the electrode Y1 forming a pair with the electrode X1, a reset pulse 1701, a scanning pulse 1702 and sustain pulses 1704 are applied. With those reset pulses 1700 and 1701, weak discharge occurs between the electrodes X1 and Y1 irrespective of occurrence of discharge in the previous sub-field, thereby developing electron in a form of the wall electric charge on the electrode X1 while ion on the electrode Y1. Next, by means of the scanning pulse 1702 on the electrode Y1 and a pulse (not shown in the figure) on the electrode A, discharge occurs between the electrode A and the electrode Y1, and this comes to be a trigger for generating the self-erase discharge between the electrode Y1 and the electrode X1. With this, the wall electric charge developed upon the reset pulse is erased (i.e., address erase). Next, though the sustain pulses 1703 and 1704 are applied onto the electrodes X1 and Y1, since no wall electric charge is remained in the display cell, no light emission occurs with this sustain pulses. When conducting the light emission for display,

no pulse is applied onto the electrode A when the scanning pulse of the electrode Y1 is applied to. In this instance, since there is remained the wall electric charge developed by the reset pulse in advance, then the operation of light emission between the electrodes X1 and Y1 by means of the sustain pulses is carried out.

Next, on the non-selection line L2 of the 2nd line, to the electrode X2 is applied the sustain pulses 1705, being same in phase to the sustain pulses 1704, which are generated from the X collector circuit 2 and applied onto the electrode Y1. Since the sustain pulses are same in the phase thereof, error light emission will never occur on the line L2. Also on the line L3, the pulse waveforms on the electrode Y2 is same to those on the electrode Y1, however since the sustain pulses on the electrodes X2 and Y2 are same in the phase, no light emission will occurs.

Next, on the line L4, to the electrode X3 are applied the sustain pulses 1705, being same in phase to the reset pulse 1700, and the sustain pulses are applied on the electrode Y2 from the X collector circuit 3. The line L4 constructed with the electrodes Y2 and X3 will never occur light emission since the sustain pulses thereof are same in phase.

Next, on the selection line L5, to the electrode Y3 are applied the reset pulse 1701, the scanning pulse 1707, and the sustain pulses 1708, which are reversed in phase opposite to the sustain pulses on the electrode X3. Those sustain pulses on the electrode Y3 are generated from a Y collector circuit 2, being different from the Y collector circuit for generating the sustain pulses onto the electrodes Y1 and Y2. In this manner, since to the electrodes X3 and Y3 are applied the reset pulse and the scanning pulse, and the sustain pulses being opposite to in phase to each other, then the electrodes X3 and Y3 are selected in a pair to form a line.

Next, onto the electrode X4 is applied the sustain pulses

1703, which are same in phase to those on the electrodes Y3 and Y4, from a X collector circuit 4, and the lines L6 and L7 are non-selection lines. Also, onto the electrode X5 are applied the reset pulse 1700 and the sustain pulses, being same in phase to those on the electrode Y4, from the X collector circuit 1. Since this electrode X5 is also connected with the electrode X1, in common, it is provided with the same pulses to those, which are applied to the electrode X1. Since the sustain pulses applied onto those electrodes X5 and Y4 are same in phase, L8 is turned to the non-section line.

Next, onto the electrode Y5 are applied the rest pulse 1701 and the scanning pulse 1709, as well as, the sustain pulses 1704 being different in phase from those on the electrode X5, and then those electrodes Y5 and X5 construct the selection line in a pair. The sustain pulses on this electrode Y5 are generated from the Y collector circuit 1.

In this manner, common connection of two (2) pieces of lines of the Y electrodes enables to cut the number of the scan ICs down to a half (1/2) thereof. The selection of lines in this case can be conducted through combination of four (4) of the X collector circuits and two (2) of the Y collector circuits.

Next, explanation will be given on a seventh embodiment of the present invention, by referring to Figs. 18 and 19. An aspect differing from the fifth embodiment lies in that at least one period of the 1st, 2nd, 3rd and 4th periods of the first and second fields is different from other sub-fields and periods in alignment order thereof. According to the display method of the present invention, since the time and line of the display are different in four (4) periods, the sub-fields are different in the alignment order in those four (4) periods, thereby enabling scattering or dispersion of the pseudo-contour in space. Accordingly, in addition to the cut-down of the display time for one display line to a half (1/2) field, also the pseudo-contour can be further reduced down.

Fig. 18 shows an example, wherein the alignment orders of sub-fields are different in 1st and 2nd phases, and 3rd and 4th phases, respectively. Plural numbers of the sub-fields are weighed by changing the number of the sustain pulses to be applied within the display period, so as control the light emission in those sub-fields, therefore the gradation can be presented by changing the number of light emission pulses weighted. Now, assuming that the number of the sub-fields is eight (8), being attached with numerical references, 1, 2, 3, 4, 5, 6, 7 an 8, respectively, and also that a ratio of weighting on the sub-fields (display time) is 1:2:4:8:16:32:64:128, then it is possible to obtain gradation display of 256 steps from the combination of light emissions in those sub-fields. In the alignment order of sub-fields, generally, the sub-field having the heaviest weight is put in a center and other sub-fields are aligned in front and/or rear thereof in such the order, that the weight comes down small gradually (i.e., the display time is shorten). It is assumed that the sub-fields are aligned, for example, 1, 3, 5, 7, 8, 6, 4, 2, in the order of alignment. As is shown in the Fig. 18, in the 1st period (1st phase) of the first field, the sub-fields are aligned in this order, however they are aligned in the order, 2, 4, 6, 8, 7, 5, 3, 1, opposing to that, in the 2nd period (2nd phase) of the first field. With such the alignments in this manner, appearance of the pseudo-contour obstruction can be made reversed in the manner thereof between the 1st and 2nd phases, i.e., in the condition of negating each other, therefore said the pseudo-contour obstruction can be reduced. Also, similarly in the 3rd and 4th phases, with reversing in the alignment orders of the sub-fields to each other, it is possible to reduce the pseudo-contour obstruction, which appears in the second field.

Fig. 19 shows other example of the alignment order of sub-fields. Other than the alignment mentioned above, as another alignment order of the sub-fields, for achieving the same effect to that, there is a manner, wherein the heavily weighted sub-fields are disposed at both ends of the alignment, while other sub-fields

are aligned in such the order, that the weight comes to be small as it comes up to the center thereof. Such the order is, for example, 8, 6, 4, 2, 1, 3, 5, 7, and so on. A four (4)-phase driving is conducted by combining those methods for the alignment, i.e., the sub-fields are aligned, so that the weight comes down smaller gradually as it comes up to the center, in one of them, while it comes up larger (heavy) gradually, and in the other thereof. In the Fig. 19, the alignment is 1, 3, 5, 7, 8, 6, 4, 2 in the 1st phase, and it is 8, 6, 4, 2, 1, 3, 5, 7 in the 2nd phase. In the case of the alignment of the 1st phase, the pseudo-contour appears in the central side of the alignment of the sub-fields, while, on the contrary to this, it appears at both sides thereof in the case of the alignment of the 2nd phase. Accordingly, the timing when the pseudo-contour obstruction appears can be dispersed between the alignments of the cases of the 1st phase and the 2nd phase, therefore it is possible to make the pseudo-contour unnoticeable. The alignment within the 3rd phase is reversed in the order of the sub-fields opposite to the alignment within the 1st phase, and that within the 4th phase is reversed in the order of the sub-fields opposite to the alignment within the 2nd phase. With such the structure as was mentioned above, it is possible to scatter or disperse the pseudo-contour appearing between two (2) of the sub-fields.

The second embodiment mentioned in the above is in a case, where the weighting is conducted by means of the binary code, however the present invention should not be restricted only to that. The present invention is also applicable to the structure of sub-fields, in which there are provided plural numbers of the sub-fields, being weighted substantially in equal, for example, 1:2:2:4:4:8:8, etc. Also, the number of the sustain pulses in the sub-field, which is weighted by the binary code, does not fit to the value obtained by the binary code, correctly, due to saturation in the brightness of fluoresce substance, the brightness of address discharge, etc., therefore, it is generally designed within an allowable error amount of about 10%, and this case is also involved within the

gist of the present invention.

Next, explanation will be given on an eighth embodiment of the present invention, by referring to Figs. 20, 21 and 22, and a Table 2, as well. An aspect differing from the fifth embodiment lies in that the three (3) phase display is conducted by one (1) field, according to the present eighth embodiment, on the contrary to this, the four (4) phase display is conducted by two (2) fields in the fifth embodiment. The same panel is used herein, as was explained in the fifth embodiment.

Explanation will be given on a display condition by referring to Fig. 20. The time of one (1) field is divided into 1st period, 2nd period, and 3rd period. In the 1st period, X(3p+1) and X(3p+2) of the display electrodes X form a display line in a pair, wherein the display is conducted by generating surface discharge between those electrodes by means of the sustain pulses. In the 2nd period, X(3p+2) and X(3p+3) of the display electrodes X form a display line in a pair, and the surface discharge is generated between those electrodes by means of the sustain pulses. In the 3rd period, X(3p+3) and X(3p+4) of the display electrodes X form a display line in a pair, and the surface discharge is generated between those electrodes by means of the sustain pulses, thereby obtaining the display.

Fig. 21 is a view for showing a method for forming the sub-fields for each of those phases. On a line of the 1st phase of the pair of the display electrodes, i.e., X(3p+1)-X(3p+2), all the sub-fields are disposed in the 1st period of one (1) field. On a line of the 2nd phase of the pair of the display electrodes, i.e., X(3p+2)-X(3p+3), all the sub-fields are disposed in the 2nd period of that one (1) field. On a line of 3rd phase of the pair of the display electrodes, i.e., X(3p+3)-X(3p+4), all the sub-fields are disposed in the 3rd period of that one (1) field. In this manner, since the sub-fields of the each phase are disposed within the period being cut down to one-third (1/3), it is possible

to suppress almost of generation of the pseudo-contour obstruction. The sub-fields of the each sub-field are weighted in the display period, and the each sub-field is constructed with the address period and the display period, in the same manner as in the fifth embodiment.

Fig. 22 shows voltages in the first one of the sub-fields in the 1st period, among those being applied onto the display electrodes and the address electrodes. To the display electrode X(3p+1) is applied voltage VX5, including a full write-in pulse 400, a bias pulse 404 and sustain pulses 402. To the display electrode X(3p+2) is applied voltage VX6, including a scanning pulse 401 superimposed on bias voltage 403 and the sustain pulses 403. The display line is formed with those display electrodes X(3p+1) and X(3p+2), and the surface discharge for display occurs upon the sustain pulses 402 and 403. On a while, to the electrode X(3p+3) between the display lines is applied voltage VX7, including a full write-in prevention pulse 1407 and sustain pulse discharge prevention DC voltage 1408. To the address electrode is applied voltage VA, including a full write-in prevention pulse 1409, an address pulse 405 and sustain pulse discharge prevention DC voltage 1411. The function of each of the pulses of those voltages, i.e., VX5, VX6 and VX7 are same to those of the VX1, VX2 and VX3 shown in the Fig. 14, which were mentioned in the fifth embodiment. However, the period of the total sub-field is a half (1/2) of the field in the case of the fifth embodiment, on the contrary to this, it further comes down to one-third (1/3) in the field in the case of this eighth embodiment. Because of this, in the case of this eighth embodiment, there is a possibility that the number of the sustain pulses for each of the sub-fields be less than that of the fifth embodiment.

A Table 2 below shows the voltages to be applied in the 1st period, the 2nd period and the 3rd period, with fourteen (14) pieces of the display electrodes X.

Table 2

	1st Period	2nd Period	3rd Period
X(1)	VX5	VX7	VX5
X(2)	VX6	VX6	VX7
X(3)	VX7	VX5	VX5
X(4)	VX6	VX7	VX6
X(5)	VX5	VX5	VX7
X(6)	VX7	VX6	VX6
X(7)	VX5	VX7	VX5
X(8)	VX6	VX6	VX7
X(9)	VX7	VX5	VX5
X(10)	VX6	VX7	VX6
X(11)	VX5	VX5	VX7
X(12)	VX7	VX6	VX6
X(13)	VX5	VX7	VX5

Next, explanation will be given on a ninth embodiment of the present invention, by referring to Fig. 23 through 26.

Fig. 23 shows the structure of the plasma display panel and the electrode driver circuits thereof, according to the present invention. In the plasma display panel 100, the display electrodes X and Y are disposed in parallel to each other, while the address electrodes A in the direction of crossing-over therewith. Because of the high definition of the display on the display panel, those pairs of the display electrodes X-Y are 1,024 in number thereof, while the address electrodes 3, 072 in common from up to down (one pixel is constructed with three (3) pieces thereof, and 1,024 pixels in horizontal direction). For the purpose of applying the scanning pulses onto the Y electrodes, those electrodes are connected to scan ICs, however the scan ICs are divided into up and down on the panel, wherein a scan IC 2300 forms one group for the electrodes from Y1 to Y512, while a scan IC 2301 for the other from Y513 to Y1024. To the scan IC for each group are connected a Y power collector circuit 1 (2302) and a Y power collector circuit 2 (2303), for

applying display sustain pulses. On a while, a driver circuit for the X electrodes comprises a X power collector circuit 1 (2304) for applying display sustain pulses to the electrodes from X1 to X512, respectively, and a X power collector circuit 2 (2305) for applying them onto the electrodes from X513 to X1024, respectively. Also, to the address electrodes A is connected an address IC, for the purpose of applying address pulses depending upon information to them, respectively.

Fig. 24 shows an example of driving operation of the plasma display panel according to the present invention. The display lines constructed with the display electrodes X-Y are divided into two (2) regions, i.e., the one group from 1st line to 512th line, and the other group from 513th line to 1,024th line. In each of the groups, one (1) sub-field is constructed with reset period of same time, blanking period(1), address period, and display period, and those periods are shifted, respectively, in time period in the other group. Herein, the feature of the present invention lies in that the display sustain operation (in the display period) is conducted on the group of the lower portion of the panel, while during this period, the address operation (in the address period) on the group of the upper portion thereof. In this manner, the address operation and the display sustain operation can be conducted at the same time, i.e., between the upper and the lower portion of the panel, and this brings about rise-up of a coefficient of use of time, as well as, realization of the display of the large number of sub-fields and application of large number of sustain pulses, thereby enabling improvement against the pseudo-contour and for display with high brightness.

Next, explanation will be given on a driving method of the panel, in more details thereof, by referring to Fig. 24. In a first sub-field (SF1) from the 1st line to the 512th line in the upper portion of the panel shown in the Fig. 24, first of all, there is provided the reset period for applying pulses for preparation of addressing. In this period, erasing is conducted on the wall

electric charge, which was developed in the last sub-field of the previous field, as well as, the discharge all over the surface of the upper portion of the panel, once, (write-in and erase on all over the surface), thereby remaining only a portion of the spatial electric charge in the discharge cells within the panel (residual spatial electric discharge), so as to be driven to discharge in the next address period, easily with low voltage. In the driving of the upper portion of the panel, there is provided a slight blanking period(1) after the reset period. This blanking period(1) is to prohibit the address period from being overlapped between the upper and lower portions of the panel. In the address period of the upper portion of the panel, the scanning pulses are applied to those lines from 1st line to 512th line, thereby conducting the scanning. In the address period of the lower portion of the panel, the scanning pulses are applied to those lines from 513th line to 1,024th line, thereby to conducting the scanning. On the scanning operation in the address period, there is provided the blanking period(1), so that the scanning is suspended or stopped there, once when it is conducted in the vicinity of a boundary portion between the upper and lower portions of the panel. This blanking period(1) is set to be same to the reset period in timing, so that the scanning is conducted in the vicinity of the boundary portion between the upper panel portion, after completion of the reset period of the lower panel portion. This is because, if the lower panel portion conducts the reset discharge on the boundary portion between the upper panel portion, the wall electric charge is disturbed on the borderline between the upper panel portion, therefore, for the purpose of prevention from this, the address discharge on the borderline between the upper panel portion is conducted after the reset discharge of the lower panel portion, so as to develop the wall electric charge with certainty. In the upper panel portion, the display period is provided after the address period, thereby bringing only the discharge cells, in which the wall electric discharges are developed within the address period, to achieve the display operation. On a while, in the driving operation of the lower panel portion, the reset period of the first

sub-field overlaps with the blanking period(1) of the upper panel portion, and the blanking period(1) is provided just after the reset period because of existence of a portion of the address period of the upper panel portion, therefore the scanning is conducted on the lines from the 1,024th line to the 513th line, in the address period after that, in direction from down to up on the panel. In this manner, the direction of scanning in the lower panel portion is opposite to that in the upper panel portion, however, with doing so, it is possible to bring the scanning operation on the panel boundary portion of the lower panel portion to be conducted after the completion of the reset period of the upper panel portion. When the scanning of the lower panel portion comes close to the boundary portion, there is provided the blanking period(1), and during of this, the reset operation is conducted in the upper panel portion. When the scanning is completed on the lower panel portion, the display is performed by applying the display sustain pulses in the display period.

Herein, in a case where the display period is long, such as the second sub-field (SF2) of the upper panel portion, the blanking period(1) provided between the address periods of the lower panel portion is elongated until when the display period and the reset period of the upper panel portion are completed.

Figs. 25 and 26 are views of showing the scanning method for achieving the same display on two (2) lines. Fig. 25 shows the scanning method on the upper panel portion, while Fig. 26 shows that on the lower panel portion. In the upper panel portion in the Fig. 25, the scanning pulses are applied at the same time to the first field, i.e., Y1 and Y2, Y3 and Y4,..., Y511 and Y512. With this, the 1st and 2nd lines, the 3rd and 4th lines,..., the 511th and 512th lines display the same on them in a pair. Because the television signal is an interlaced signal, therefore, two (2)-line display is performed with the signals separated by every second line. In the second field, in a manner of stitching between the simultaneous displays of two (2) lines of the first field, the

scanning pulses are applied onto the electrodes, Y2 and Y3, Y4 and Y5,..., Y510 and Y511, and Y512, at the same time, thereby making the 2nd and 3rd lines, the 4th and 5th lines,...display the same on them in a pair. With doing so, the displayed picture is improved in quality thereof. Fig. 26 shows the scanning method of the lower panel portion. The scanning is directed from the 1,024th line to the 513th line, and the scanning pulses are applied onto the electrodes, Y1024 and Y1023,..., and Y514 and Y513, at the same time. Also, in the second field, the scanning pulses are applied onto the electrodes, Y1024, Y1023 and Y1022,..., Y515 and Y514, and Y513, at the same time.

Herein, comparison is made between the conventional art and the present invention, in particular, on a ratio of utilization of time. It is assumed that the number of display lines is 1,024, the same display is conducted on two (2) lines, and the address period (width of the scanning pulse) is 2 μs, for both the conventional art and the present invention. A Table 3 below is for the purpose of comparison of the utilization of time, between the conventional art and the present invention.

Table 3

Item	Present Invention	Conventional Art
Number of Sub-fields	12	12
Address Period (μs)	2	2
Reset Period (ms)	1.9	1.9
Address Period (ms)	6.1	12.2
Display Period (ms)	4.3	2.5
Blanking period(1) (ms)	1.9	0
Blanking period(2) (ms)	2.4	0

With the results mentioned above, any case thereof is calculated out by assuming that the ratio of the display period

is 1:2:4:8:16:32:32:32:32:32:32:32 in the twelve (12) sub-fields. Also, the waiting time means the time from the end of display period to the reset period of the present invention, and this is a time zone for adjusting the address periods between the upper and lower panel portions, not so as to be overlapped with each other. Apparent from the above table, the display period is elongated to be about 1.7 times long in the present invention, comparing to that of the conventional art, and then, much large number of display sustain pulses can be applied to, for it. Therefore, in the present invention, the brightness can be obtained about 1.7 times higher, comparing to that of the conventional art.

Next, explanation will be given on a tenth embodiment of the present invention, by referring to Figs. 27 and 28.

Fig. 27 shows the structure of providing a horizontal rib 2700 at the boundary portion between the upper and lower panel portions, for the purpose of cutting the movement of electric charges between the discharge cells. For preventing stroke from occurring on the boundary portion between the upper and lower panel portions, according to the ninth embodiment, the blanking period(1) is provided in each sub-field, and the scanning direction is reversed in the lower panel portion, so that the scanning of the line on the boundary portion comes after the end of the reset period. On the contrary to this, because the horizontal rib is provided at the boundary portion, in the tenth embodiment, it enables to prevent the stroke from occurring between the discharge cells, therefore there is no necessity of providing the blanking period(1) or the reverse scanning. Because the blanking period(1) can be removed therefrom, the display period can be elongated for it, and much large number of the display sustain pulses can be applied to. Because of this, the display can be brightened much more than the case of the ninth embodiment mentioned above.

Fig. 28 is a view for showing a driving method of the panel with provision of the horizontal rib at the boundary portion of

the panel. An aspect differing to that shown in the Fig. 24 lies in that the blanking periods, provided after the reset period and on the way of thereof, are removed, and that the scanning in the lower panel portion is made to direct from the 513th line to the 1,024th line. In this case, also the display being same on two (2) lines is also conducted, and the method of applying the scanning pulses is same to the case as was shown in the Fig. 25. The Fig. 26 shows the reverse scanning of the ninth embodiment, however it is not necessary in the tenth embodiment, any more.

Next, explanation will be given on an eleventh embodiment.

In the ninth and tenth embodiments, the panel is divided into the upper and lower portions, and then the display periods and the address periods are superimposed between the both upper and lower portions thereof, in time. With this driving method, since the address electrodes are wired round on upper and lower sides of the panel, in common, it may happen a case that leakage voltage of the sustain pulses may appear on the address pulse, due to capacitive connection between the address electrodes and X-Y display electrodes, when the display sustain pulses are applied in the upper panel portion.

In such the case, there is possibility that error occurs in the address operation. This eleventh embodiment shows a method for applying pulses, which may causes such the error mentioned. Fig. 29(a) shows waveforms of the display sustain pulses and the address pulses on the X-Y display electrodes. In a case where the X-Y display electrodes and the address electrodes form the capacitive connection therebetween, the leakage voltage 2900 appears on the address electrode during transition period in the voltage of the sustain pulse. In this case, the leakage voltage appears as a noise, however the sustain pulse and the address pulse are adjusted in the phase therebetween, so that the time of appearing this noise comes within voltage hold period of the address pulse. Fig. 29(b) shows a representative one of the address voltage driver

circuit, and is generally of a push-pull type. The address pulse sometimes contains pulses or not, depending upon information, however there is necessarily provided the transition period between them when the pulses are applied thereto. This transition period lies when an upper FET 2903 or a lower FET 2904 starts turning ON thereof, and at that instance an output impedance of the circuit comes to be large value. When the leakage voltage, due to the capacitive connection, enters into or appears on the address electrode from the X-Y electrodes, the noise thereon comes to be large. If the leakage voltage appear when the FET 2903 or FET 2904 is fully turned ON, it passes through the FET 2903 or a parasitic diode 2901 thereof, or the FET 2904 or a parasitic diode 2902 thereof, and flows into a direction of a power source of the leakage voltage, therefore the noise appearing on the address electrode comes to be small. In this manner, shifting of the transition period on the display sustain pulse to be applied to the X-Y electrodes within the hold period of the address pulse, enables address operation without the error in operations thereof. This method can be realized by adjusting the phase of either one, when the address pulse and the sustain pulse are in a relationship that can be expressed by a ratio of integer between the periods thereof.

Next, detailed explanation will be given on a twelfth embodiment of the present invention, by referring to Figs. 30 through 33.

Fig. 31 shows the condition of address discharge in the conventional art. When the scanning pulse 3104 and the address pulse, each having pulse width "ts", are applied onto the Y electrode and A electrode, discharge is generated between the address electrode and the Y electrode with a time delay of "td", wherein current 3103 flows out on the address electrode while current 3102 flows in on the Y electrode. Triggering of this discharge, another discharge is generated just after thereof between the X electrode and the Y electrode, thereby causing the flow-out of current 3100 on the X electrode while the flow-in of current 3101 on the Y electrode.

The X electrode and the Y electrode are covered with dielectric substance, therefore the wall electric charge is developed due to the discharge, and the discharge is stopped when the substantial voltage, i.e., the sum of the voltage applied and the voltage caused due to the wall electric charge, comes down to be lower than discharge sustain voltage. This is the time indicated by "tm" in the figure, and this series of the address discharges are conducted within a period during when the scanning pulse is applied to. Accordingly, there is established a relationship, i.e., $tm \leq ts$. The time "tm", indicating the time period until when this address is ended, depends largely on the structure of the panel, such as, sizes of the discharge cell, a mixture ration of Ne-Xe gas, pressure of the gas, width of the electrode, properties of MgO film, etc., and the time "tm" must be equal to 1 μs or larger than that, according to the present technology of manufacturing the panel.

Fig. 30 shows waveforms of the scanning pulse to be applied onto the scanning electrode, i.e., the Y electrode, and discharge voltages on the respective electrodes. This is characterized that the width "ts" of the scanning pulse is shorter than the time "tm" until the end of the address discharges. When applying the scanning pulse 3000 onto the Y electrode while the address pulse 3006 onto the address electrode, discharge is caused between the address electrode and the Y electrode after delaying by the discharge time "td", and the current flow-out appears on the address electrode while the current flow-in on the Y electrode. Being triggered with this discharge between the address electrode and the Y electrode, the discharge is generated between the X electrode and the Y electrode, and the current flow-out appears on the X electrode while the current flow-in on the Y electrode. During the time perioid when the discharge is generated between the X electrode and the Y electrode, the scanning pulse is ended, and then voltage rises up. At that instance, the discharge between the X electrode and the Y electrode becomes weak, so that the discharge current is decreased, however the voltage 3001 applied onto the Y electrode

just after the scanning pulse sustains the discharge between them. In that instance, the discharge continues or is sustained between the X electrode and the Y electrode if the scanning pulse is ended, therefore discharge current 3002 flows on the X electrode and discharge current 3003 on the Y electrode, continuously. With those sustain discharge currents 3002 and 3003, the wall electric charge is developed, sufficiently, between the X electrode and the Y electrode, as a memory medium. Those sustain discharge currents 3002 and 3003, however, stop when the sum of electric fields comes down to equal or greater than the discharge sustain voltage, i.e., the one developed by the voltage applied onto the X electrode and the voltage 3001 applied onto the Y electrode, and other due to the wall electric charge developed between the X and Y electrodes.

Pulses 3009 of information on other display line is also applied onto the address electrode, however no discharge is caused between voltage of the pulse 3009 on the address electrode and the voltage 3001 after the scanning pulse on the Y electrode. This is because the voltage 3001 is set up so that no discharge is generated between the voltage after the scanning pulse and the voltage of the address pulse, even if occurring discharge between the voltage of the scanning pulse and the address pulse. Also, that voltage 3001 is set up, so that the sustain discharge of the address discharge is generated between the X electrode and the Y electrode. It is possible to set up the value of this voltage with satisfying both those conditions, since the difference between the voltage value for keeping the sustain discharge and the value of discharge start voltage lies in a range from several tens to a hundred V or the like. Also, the sustain discharge is kept between the X electrode and the Y electrode, and the discharge sustain voltage between the both electrodes, according to the present panel characteristics, is lower than that in the case of discharging between the address electrode and the Y electrode.

Fig. 32 shows waveforms of the driving voltages on the X electrode, the Y electrode and A electrode (i.e., the address

electrode), respectively. After applying the reset pulse 400 onto the X electrode in the address period, the bias pulse 404 is applied onto the X electrode while applying the scanning pulse 3200 and the voltage 320 for sustaining the address discharge onto the Y electrode as the scanning electrode. In this example, the voltage 3201 is applied to during all the time of the address period. Applying the address pulse 405, depending upon information, onto the A electrode, discharge is generated between the address electrode and the Y electrode when the address pulse 405 and the scanning pulse overlap each other. With triggering of this, another charge occurs between the X electrode and the electrode, and this discharge continues in the form the sustain discharge by the voltage 3201 after the end of the scanning pulse 3200. In the display period after the address period, alternating sustain pulses 402 and 403 are applied between the X electrode and the Y electrode, thereby making only the discharge cell, in which the wall electric charge is developed through the address discharge in the address period, emit the light for display.

Fig. 33 shows another example of waveforms of the scanning pulses and voltages, to be applied to the Y electrodes during the address period. The Yn electrode (i.e., the Y electrode of Yn^{th} number) is set from the ground voltage 3303 to such voltage that it sustain no address discharge in the address period, and then the scanning pulse 3301 is applied thereto. And, it is set to such voltage that it sustains the address discharge, just after completion of application of the scanning pulse 3301. This voltage 3302 is applied until when the sustain discharge of the address discharge is fully ended, and thereafter, it is increased up to the level of voltage 3300 which causes no sustain discharge. After completing the address period, it is turned back to the ground voltage 3303, again, and in the display period after that, the sustain pulse is applied to. The voltage 3302 for sustaining the address discharge is delayed in the application time, sequentially, in the same manner of the scanning pulse, on the Yn+1 electrode. In this way, provision of the level of voltage 3300 causing no

sustain discharge therewith enables the prevention of the error discharge from occurring between the address pulse on the address electrode.

In this manner, the scanning pulse is ended before the address discharge is finished, and sustain discharge is caused thereafter, and this enables to make the width of scanning pulse narrow. In this case, the width of the scanning pulse is set to a value, so that the scanning pulse rises up after starting the discharge between the X electrode and the Y electrode, which is triggered by discharge between the address electrode and the Y electrode. Since the delay of discharge between the address electrode and the Y electrode is about 0.5 μs, and the transition period of discharge between the X electrode and the Y electrode is achieved, momentarily, the width of the scanning pulse can be set to a value from 0.5 μs to 1.0 μs. Assuming that the scanning pulse width is set to 0.75 μs, for example, the address period in a one (1) sub-field comes to be 0.75 ms in the HDTV plasma display television apparatus having display lines more than 1,000, while the address period of the one (1) sub-field 900 μs (= 150 μs + 0.75 μs × 1,000), including the reset period of 150 μs. The sum of all the address periods when driving the twelve (12) sub-fields is 10.8 ms (= 900 μs × 12), and the display period can be taken for 5.9 ms (= 16.7 ms - 10.8 ms). As a result of this, assuming that the period of the sustain pulse is 6.0 μs, the number of the sustain pulses of one (1) sub-field is about 980 (5.9 ms ÷ 6.0 μs), this means the sustain pulses can be applied with the number thereof as two times (×2) large as the conventional art, thereby improving the brightness greatly.

According to the present invention, the following effects can be achieved:

(1) Conducting same display on two (2) lines by applying

the scanning pulses of same phase while achieving the interlace display by shifting one (1) line between the first field and the second field enables the display of a large number of sub-fields, thereby obtaining high gradation display with fully taking measures against the pseudo-contour.

(2) Forming the display cells (lines) with all spaces defined between the neighboring parallel display electrodes, dividing the display lines into plural numbers of phases, i.e., three (3) phases or more, and separating display periods within one (1) field for each the phase, obtains a plasma display apparatus of high picture quality, with high definition panel but having less pseudo-contour thereon.

(3) Since the driving is performed, so that the address periods and the display periods overlap each other on both sides of the panel, therefore the coefficient of use or utilization factor of time is superior, and since a larger number of display sustain pulses can be applied, there can be obtain an effect of displaying with high brightness. Also, since the address electrodes are wired on both sides of the panel in common, address electrode driver circuits can be lowered in number thereof, thereby obtaining an apparatus of low cost.

(4) Sustaining the address discharge, continuingly, by means of the voltage between the Y electrode and the X electrode after completion of the scanning pulse, makes the scanning pulse narrow, therefore it is possible to obtain the display with high brightness, with high gradation driving measured against the pseudo-contour, on the plasma display apparatus of high definition, such as the HDTV.

INDUSTRIAL APPLICABILITY

As was mentioned in the above, the display technology according to the present invention is useful for a plasma display

apparatus, a television apparatus or receiver set, a display device for a personal computer, a display device for a game machine, etc., and is suitable, in particular, for the display apparatus of displaying the screen of large number of lines, like the high definition television apparatus (i.e., HDTV).

C L A I M S

1. An display apparatus, for conducting video display through address operation on display lines upon basis of a video signal, wherein:

scanning pulses of same phase are applied to plurality of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to plurality of second display lines in a second field thereof, thereby conducting the address operation.

2. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

scanning pulses of same phase are applied to the X electrodes of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to the Y electrode of second display lines in a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

3. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

scanning pulses of same phase are applied to plural numbers of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to plural numbers of second display lines,

neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

4. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

said X and Y electrodes are disposed in reversed in the order thereof on display lines neighboring to each other;

scanning pulses of same phase are applied to the X electrodes of plural number of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to the Y electrodes of plural numbers of second display lines, neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

5. An display apparatus, as defined in the claim 1, claim 2, claim 3, or claim4, wherein voltage values of the address pulses applied to said first field and said second field.

6. An display apparatus, comprising parallel display electrodes X(i) (i = 1 through n (n: a positive number), an electrode of i^{th} number), and address electrodes A(j) (j = 1 through k (k: a positive number), an electrode of j^{th} number), being separated and crossing over said display electrodes X(i),wherein:

conducting light emission display on the display electrodes X(4p+1) and X(4p+2) (p: a positive number including zero (0)), in a first period of a first field;

conducting light emission display on the display electrodes

X(4p+3) and X(4p+4), in a second period of the first field;

conducting light emission display on the display electrodes X(4p+2) and X(4p+4), in a third period of a second field; and

conducting light emission display on the display electrodes X(4p+4) and X(4p+5), in a fourth period of the second field.

7. An display apparatus, as defined in the claim 6, wherein the said first, second, third and fourth periods are divided into plural numbers of sub-fields, respectively, and said sub-field includes an address period for applying a scanning pulse to at least one display electrode of a pair of the display electrodes X, so as to conduct write-in discharge depending upon video information between the address electrodes A, and a display period for sustaining discharge by means of wall electric charge developed in said address period.

8. An display apparatus, as defined in the claim 7, wherein alignment orders of the plural numbers of sub-fields formed within said first, second, third and fourth periods are different in at least one of said first, second, third and fourth periods.

9. An display apparatus, as defined in the claim 7, wherein a full write-in pulse, for making all discharge cells to conduct the write-in discharge, is applied onto one of the display electrodes X forming said pair, in advance to a period during when the write-in discharge is conducted in at least one sub-field of said plural numbers of sub-fields, while a voltage pulse of causing no full write-in discharge is applied at least one of those of the display electrodes X other than the above.

10. An display apparatus, as defined in the claim 7, wherein at least two (2) of the display electrodes to be applied with said scanning pulses thereon are connected in common, and the display electrodes neighboring with said display electrode are driven with

outputs having different waveforms.

11. An display apparatus, comprising parallel display electrodes X(i) (i = 1 through n (n: a positive number), an electrode of i^{th} number), and address electrodes A(j) (j = 1 through k (k: a positive number), an electrode of j^{th} number), separately crossing over said display electrodes X(i), wherein:

forming a pair with the display electrodes X(3p+1) and X(3p+2) (p: a positive number including zero (0)), and conducting light emission display on the display electrodes of said pair, in a first period of a field;

forming a pair with the display electrodes X(3p+2) and X(3p+3) and conducting light emission display on the display electrodes of said pair, in a second period of the field; and

forming a pair with the display electrodes X(3p+3) and X(3p+4) and conducting light emission display on the display electrodes of said pair, in a third period of the field.

12. A display apparatus, constructing a display screen by disposing discharge cells in a matrix-like manner, each discharge cell being constructed with a pair of display electrodes being parallel to each other and covered with a dielectric body, and with a set of an address electrode being disposed in a direction of crossing thereover, wherein:

address electrodes are disposed in common for a first panel portion and a second panel portion, constructing said display screen therewith;

operating address operation, sequentially, all said discharge cells of said first panel portion, by scanning one of the pair of display electrodes of said first panel portion, sequentially, while applying a selection pulse between the display

electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said first panel portion of said discharge cells being operated by the address operation, simultaneously, thereby conducting display sustain operation; and

operating address operation, sequentially, all said discharge cells of said second panel portion, by scanning one of the pair of display electrodes of said second panel portion, sequentially, while applying a selection pulse between the display electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said second panel portion of said discharge cells being operated by the address operation, simultaneously, thereby conducting display sustain operation; and further having:

a time band, during which the address operation of said first panel portion and the display sustain operation of said second panel portion coincide with each other.

13. A display apparatus, as defined in the claim 12, further comprising a reset period for applying a pulse for address preparation prior to said address operations of said first and second panel portions, and a blanking period for interrupting the address operation on said first panel portion at same time of the reset period of said second panel portion.

14. A display apparatus, as defined in the claim 13, wherein the scanning of the display electrodes of one of said first and second panel portions is conducted, sequentially, in a direction of approaching to a boundary between said first and second panel portions, and time when conducting the scanning in vicinity of said boundary of said first panel portion is after completion of the reset period of said second panel portion.

15. A display apparatus, as defined in the claim 12, wherein

the scanning on said first and second panel portions is conducted, by conducting same display on two (2) lines with application of the scanning pulses of same time to one of the display electrodes of each of two of said pairs of the display electrodes neighboring with each other, in a first field, while conducting same display on two (2) lines with application of the scanning pulses of same time to one of the display electrodes of each of two of said pairs of a combination differing from the two of said pairs of display electrodes neighboring with each other, in a second field.

16. A display apparatus, as defined in the claim 12, wherein a rib is formed on a border between said first panel portion and said second panel portion, for cutting off movement of discharging electric charge caused between said discharge cells of said first and second panel portions in vicinity of said boundary.

17. A display apparatus, as defined in the claim 12, wherein voltage transition period of the alternating sustain pulses, which are to be applied to the pair of electrodes by the display sustain operation of said second panel portion, is included within a voltage hold period of the address pulse to be applied to said address electrode by the address operation of said first panel portion.

18. A display apparatus, having at least plural numbers of parallel scan electrodes and plural numbers of parallel address electrodes crossing over said scan electrodes separately, wherein discharge cells are formed at intersection points of said scanning electrodes and said address electrodes, and said discharge cells are disposed in a matrix-like manner, wherein:

applying scanning pulse to said scanning electrode for conducting line selection, applying address pulse depending upon information onto said address electrode, and applying voltage for sustaining said address discharge after completion of application of said scanning pulse, onto the scan electrode just after completion of said scanning pulse, in the address operation for

conducting write-in by causing the address discharge which is caused by said scanning pulse and said address pulse.

19. A display apparatus, as defined in the claim 18, wherein the voltage for sustaining said address discharge has a voltage value of causing no discharge between said scan electrodes and said address electrode by voltage of said address pulse together with.

20. A display apparatus for performing video display on display lines by operating address operation upon basis of a signal, wherein:

operating an address operation on plural numbers of first display lines upon basis of a same information, in a first field constructing one (1) frame, and operating an address operation on plural numbers of second display lines upon basis of the same information, in a second field thereof.

21. A video display method for performing video display on display lines by operating address operation upon basis of a signal, wherein:

after applying a scanning pulses of same phase onto plural numbers of first display lines upon basis of a same information, in a first field constructing one (1) frame, then, address operation is conducted by applying the scanning pulses of same phase onto plural numbers of second display lines in a second field thereof.

22. A video display method for performing video display on display lines by operating address operation based on a signal, wherein:

after operating an address operation on plural numbers of first display lines with same information, in a first field constructing one (1) frame, then, operating the address operation

on plural numbers of second display lines with the same information, in a second field thereof.

23. A video display method for performing video display by using plural numbers of display lines, wherein:

the video display is performed by dispersing said plural numbers of display lines on plural numbers of time bands obtained from one (1) frame by dividing it into three (3) or more.

24. A video display apparatus, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing a display line and an address electrodes which crosses over said display electrodes, wherein:

an address electrode is provided being connected in common to a first panel portion and a second panel portion, and an address period of a sub-field in said first panel portion and a display period of a sub-field in said second panel portion overlap with each other.

25. A video display apparatus, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing first and second display lines and an address electrodes which crosses over said display electrodes, comprising:

means for conducting same address operation by applying scanning pulses of same phase to said first display line of plural number of display lines, and a driver portion for driving plural numbers of display electrodes with driving pulses differing from each other.

26. A video display apparatus, as defined in the claim 25, wherein said driving pulses are different in phases thereof between

said second display electrodes.

27. A video display apparatus, as defined in any one of the claims 1 through 20, and 24 through 26, wherein said video display apparatus is a plasma display apparatus.

Fig. 1 Scan IC Scan IC Sustain Driver Scan IC Scan IC Scan IC Sustain Driver

Fig. 2

Fig. 3 Scan IC Scan IC Scan IC Scan IC Sustain Driver Sustain Driver

Fig. 4 Fig. 5 Fig. 6

First Field Second Field 1st Line 2nd Line 3rd Line 4th Line 5th line 6th line 7th line

Fig. 7 XY/XY Type XY/YX type

Fig. 8 First Field Second Field

Fig. 9 Scan IC Scan IC Scan IC Sustain Driver Sustain Driver Scan IC Scan IC

Fig. 10 Scan IC Scan IC Scan IC Scan IC Scan IC Scan IC Sustain Driver Sustain Driver

Fig. 11 First Field Second Field

Fig. 12 1st Period of 1st Field 2nd Period of 1st Field 3rd Period of 2nd Field 4th Period of 2nd Field 1st Phase 2nd Phase 3rd Phase 4th Phase

Fig. 13 1st Field 2nd Field 1st Period 2nd Period 3rd Period 4th Period

X(4p+1)-X(4p+2)th (1st Phase)

X(4p+2)-X(4p+3)th (2nd Phase)

X(4p+3)-X(4p+4)th (3rd Phase)

X(4p+4)-X(4p+5)th (4th Phase)

Fig. 14

Fig. 15 Video Signal Converter Field Memory Control Signal Generator Circuit Scan-sustain Driver A Scan-sustain Driver B Address Driver A Address Driver B Sustain Driver A Sustain Driver B

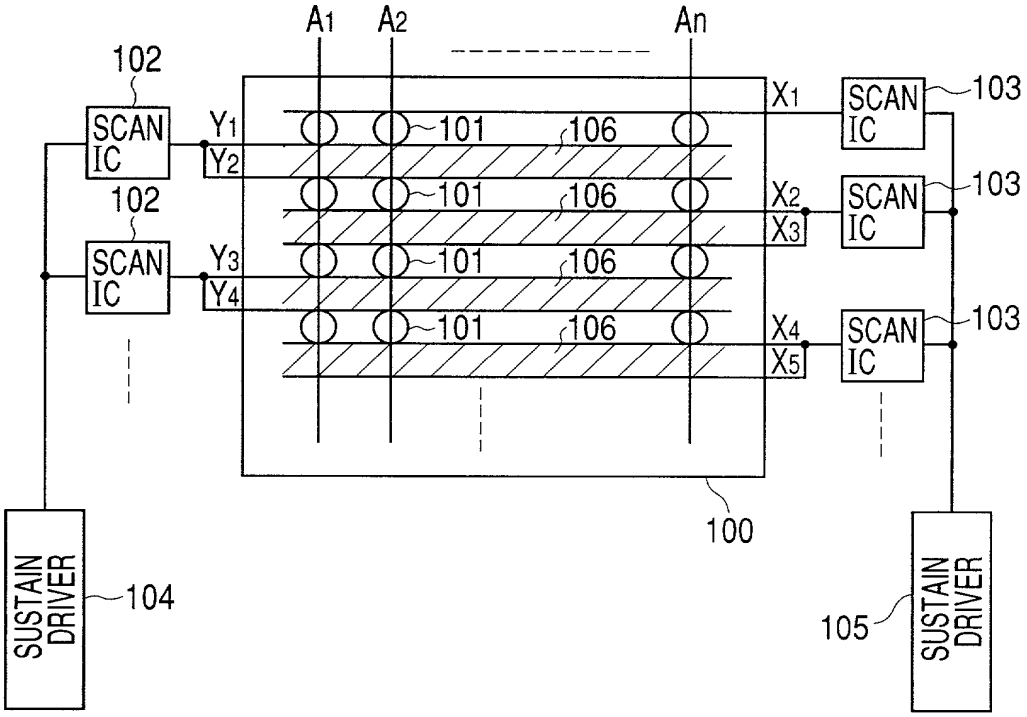
Fig. 16 Y Collector Circuit 1 Y Collector Circuit 2 Scan IC Scan IC Scan IC X Collector Circuit 1 X Collector Circuit 2 X Collector Circuit 3 X Collector Circuit 4

Fig. 17 L1(Select) L5(Select) L9(Select)

Fig. 18 First Field Second Field
1st Period 2nd Period 3rd Period 4th Period Alignment of SF
Alignment of SF Alignment of SF Alignment of SF
Fig. 19 First Field Second Field
1st Period 2nd Period 3rd Period 4th Period Alignment of SF
Alignment of SF Alignment of SF Alignment of SF
Fig. 20 1st Period 2nd Period 3rd Period
Fig. 21 First Field
1st Period 2nd Period 3rd Period
X(3p+1)-X(3p+2)th (1st Phase) X(3p+2)-X(3p+3)th (2nd Phase)
X(3p+3)-X(3p+4)th (3rd Phase)
Fig. 22
Fig. 23 Y Electric Power Collector Circuit 1 Scan IC Scan IC
Y Electric Power Collector Circuit 2 Scan IC Scan IC
X Electric Power Collector Circuit 1
X Electric Power Collector Circuit 2
Fig. 24 Field Line Line
Reset Period Hold Scanning Direction Address Period
Blanking period(1) Display Period Blanking period(2) Reset
Period
Hold Scanning Direction Address Period Blanking period(1)
Display Period Reset Period Blanking period(1) Scanning
Direction
Address Period Blanking period(1) Display Period
Blanking period(1) Address Period Display Period
Reset Period Blanking period(1) Scanning Direction Address
Period
Blanking period(1) Display Period Blanking period(2) Reset
Period
Blanking period(1) Scanning Direction Address Period
Display Period Reset Period Blanking period(1) Scanning
Direction
Address Period
Fig. 25 (1st Field) (2nd Field)
Fig. 26 (1st Field) (2nd Field) Fig. 27
Fig. 28 Line Line

Reset Period Scanning Direction Address Period
Display Period Blanking period Reset Period Scanning Direction
Address Period Display Period
Blanking period Reset Period Scanning Direction
Address Period Display Period Blanking period(1) Reset Period
Scanning Direction Address Period Display Period
Reset Period Scanning Direction Address Period Display Period
Fig. 29(a) Fig. 29(b) To A Electrode
Fig. 30 Y Voltage Waveform X Current Waveform Y Current Waveform
A Current Waveform A Voltage Waveform
Fig. 31 Y Voltage Waveform X Current Waveform Y Current Waveform
A Current Waveform A Voltage Waveform
Fig. 32 Fig. 33 Yn Voltage Waveform 33 Yn+1 Voltage Waveform

FIG. 1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A2
An
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SCAN IC
Y1
Y2
102
SCAN IC
Y3
Y4
101
106
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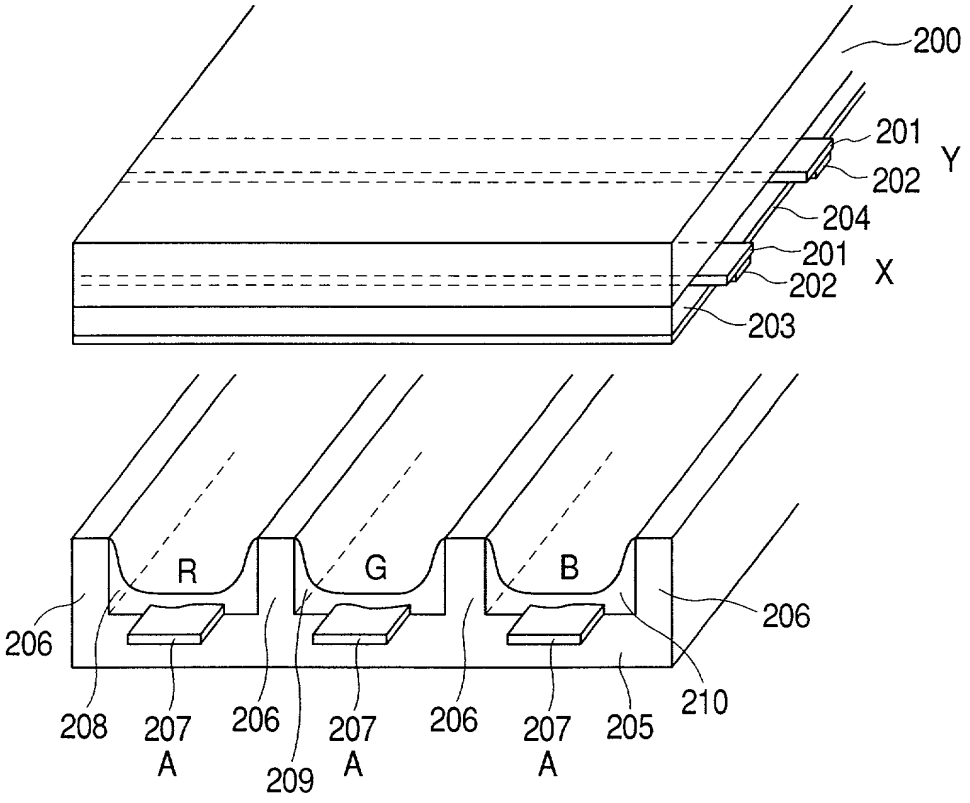
X2
X3
X4
X5
SCAN IC
103
100
SUSTAIN DRIVER
104
105
SUSTAIN DRIVER

FIG. 2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201
202
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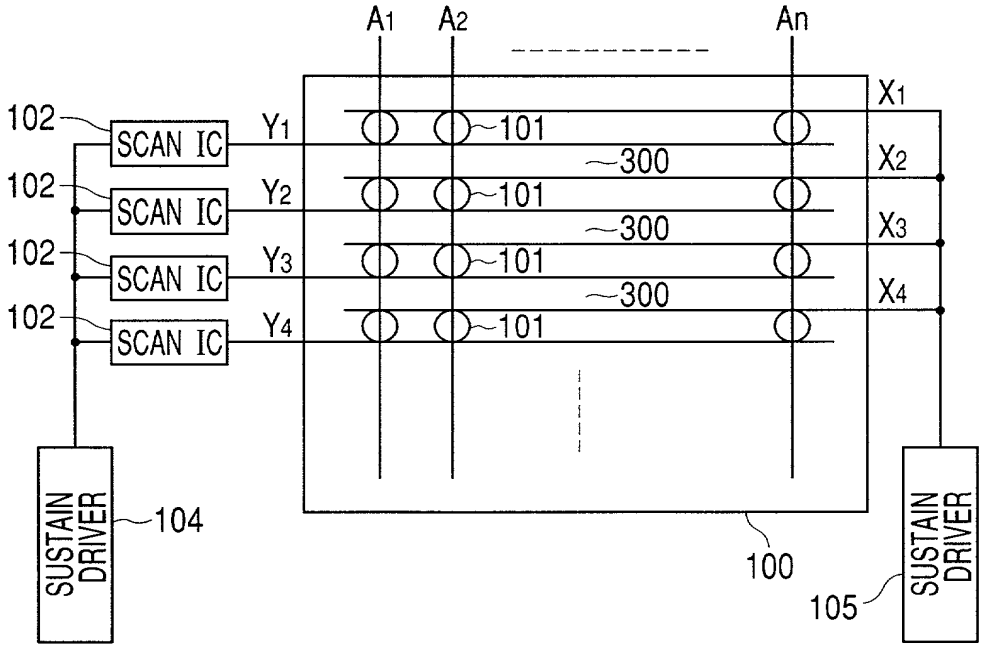
206
207
A
205
210

FIG. 3


A1
A2
An
X1
X2
X3
X4
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Y3
Y4
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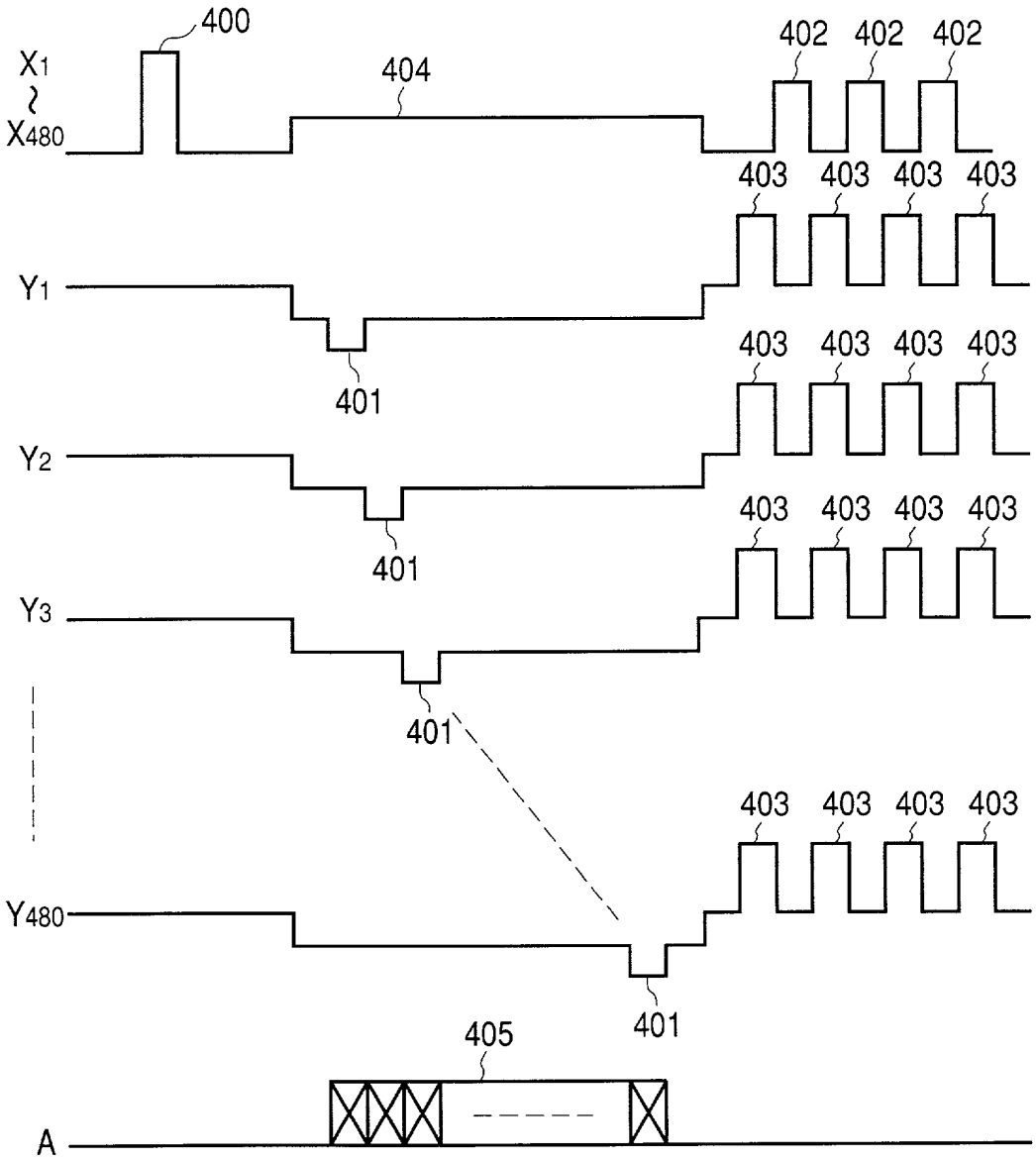
300
SUSTAIN DRIVER
104
100
105
SUSTAIN DRIVER

FIG. 4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X1
~
X480
404
402 402 402
403 403 403 403
Y1
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Y2
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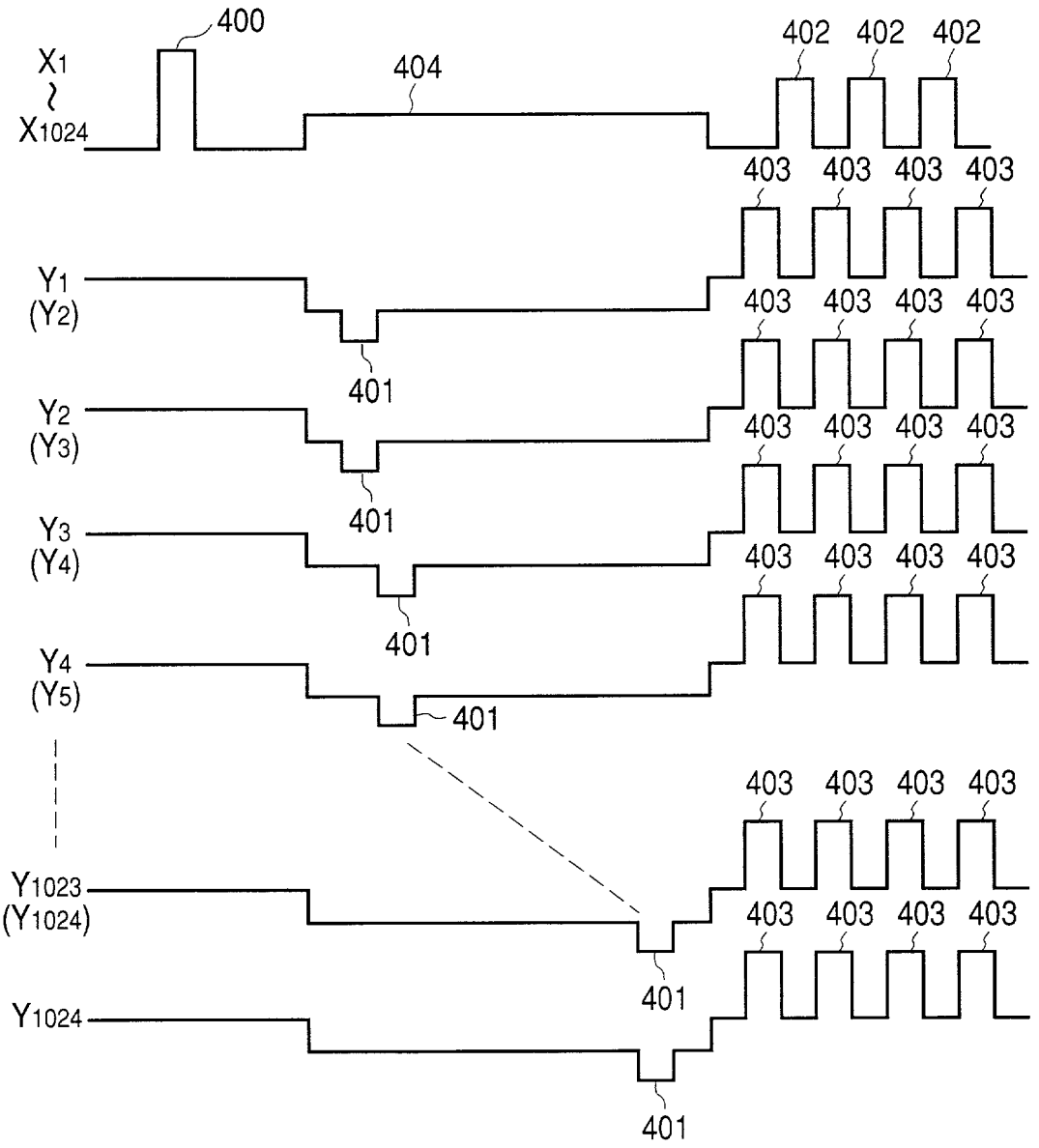
Y3
401
403 403 403 403
Y480
401
405
A

FIG. 5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Y1
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Y3
(Y4)
401
403 403 403 403
Y4
(Y5)
401
403 403 403 403
Y1023
(Y1024)
401
403 403 403 403
Y1024
401

FIG. 6

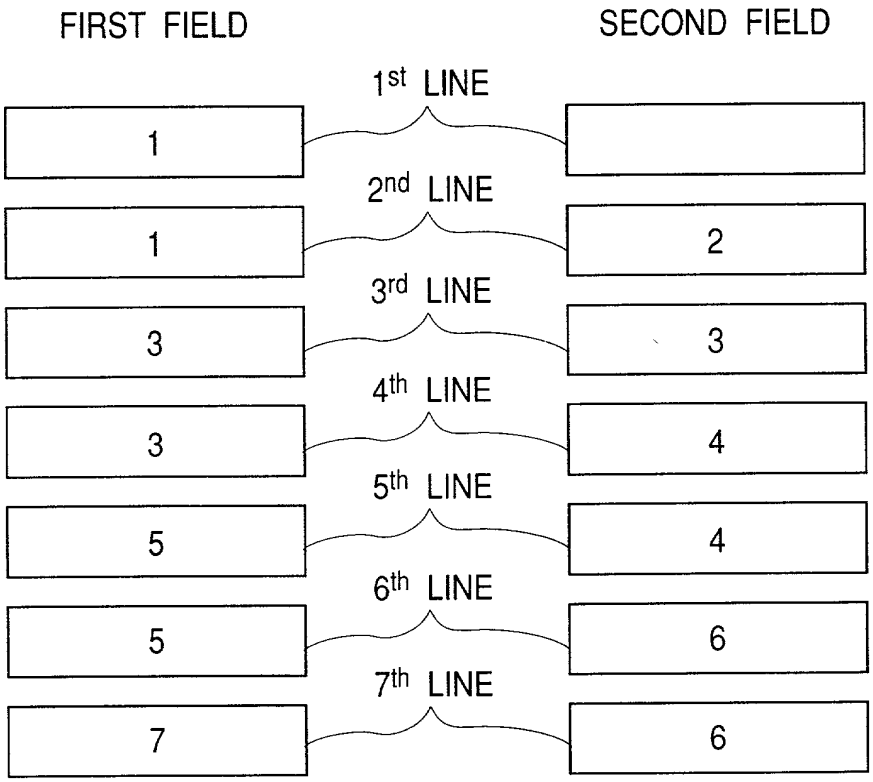
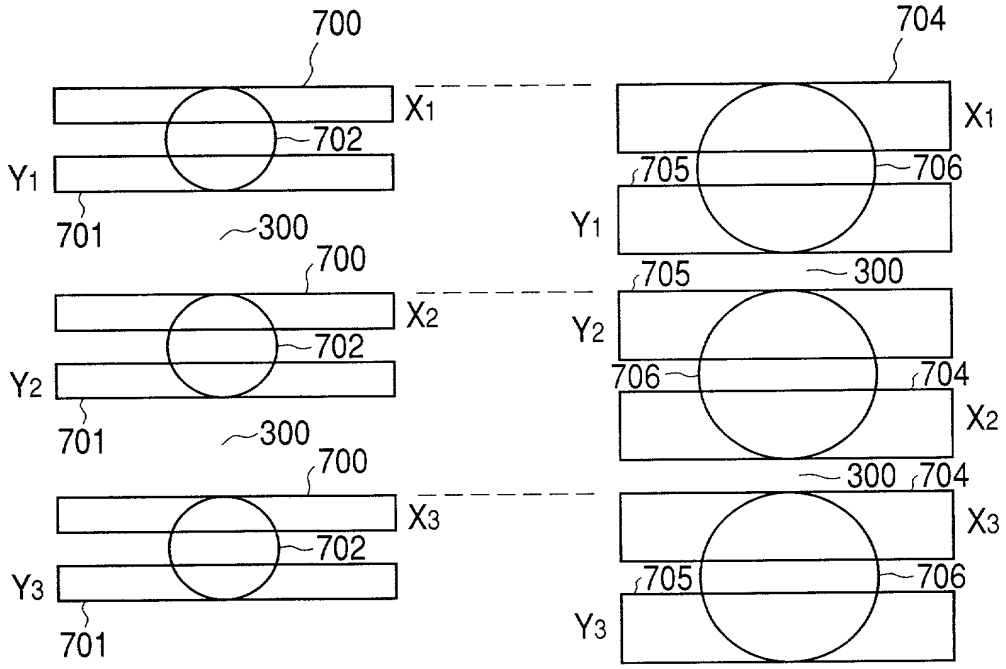

FIRST FIELD
SECOND FIELD
1st LINE
1
2nd LINE
1
2
3rd LINE
3
3
4th LINE
3
4
5th LINE
5
4
6th LINE
5
6
7th LINE
7
6

FIG. 7



(a) XY/XY TYPE

(b) XY/YX TYPE

FIG. 8

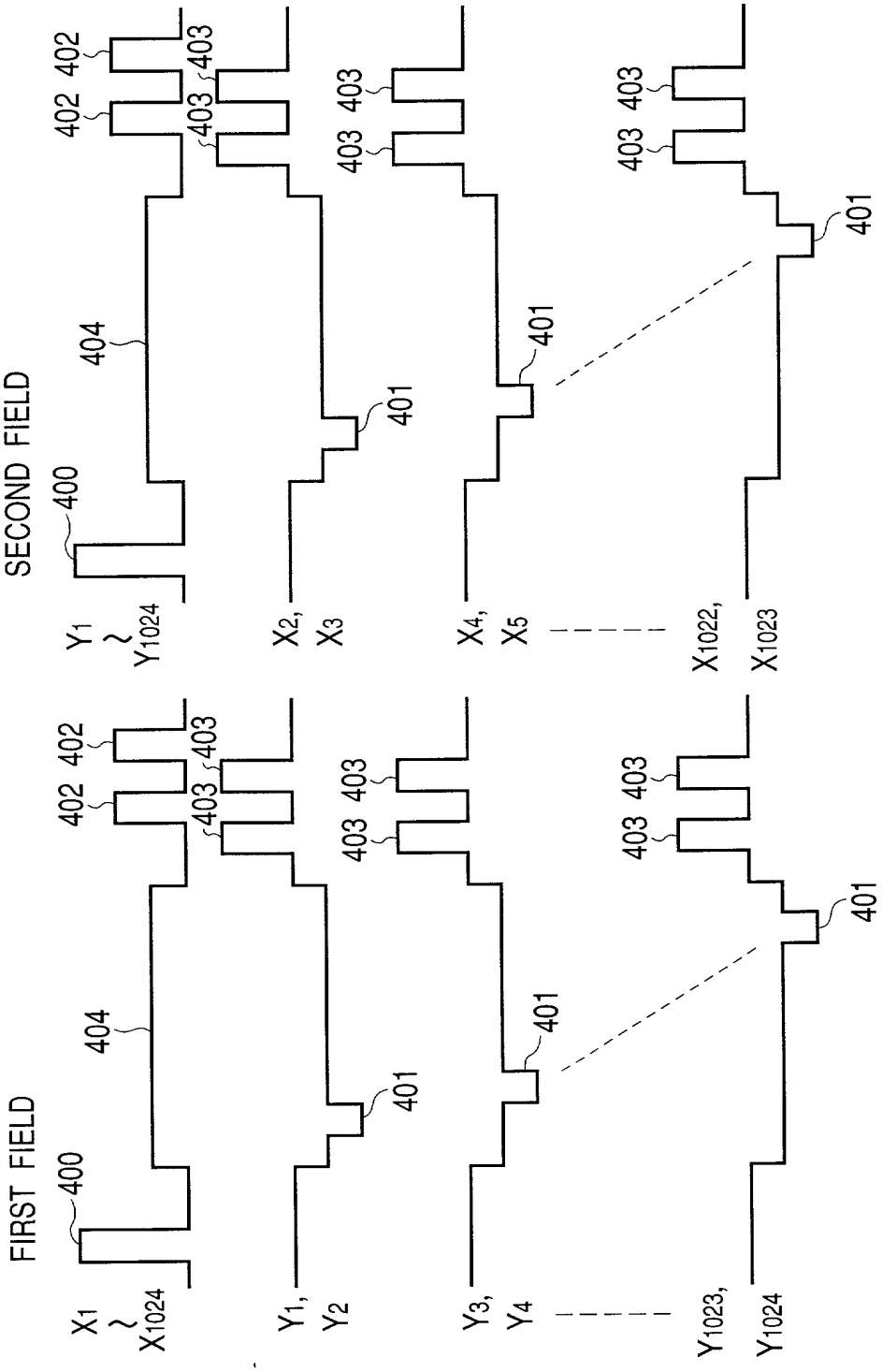

FIRST FIELD
SECOND FIELD
400
401
402
403
404
X1 ~ X1024
Y1 ~ Y1024
Y1, Y2
X2, X3
Y3, Y4
X4, X5
Y1023, Y1024
X1022, X1023

FIG. 9

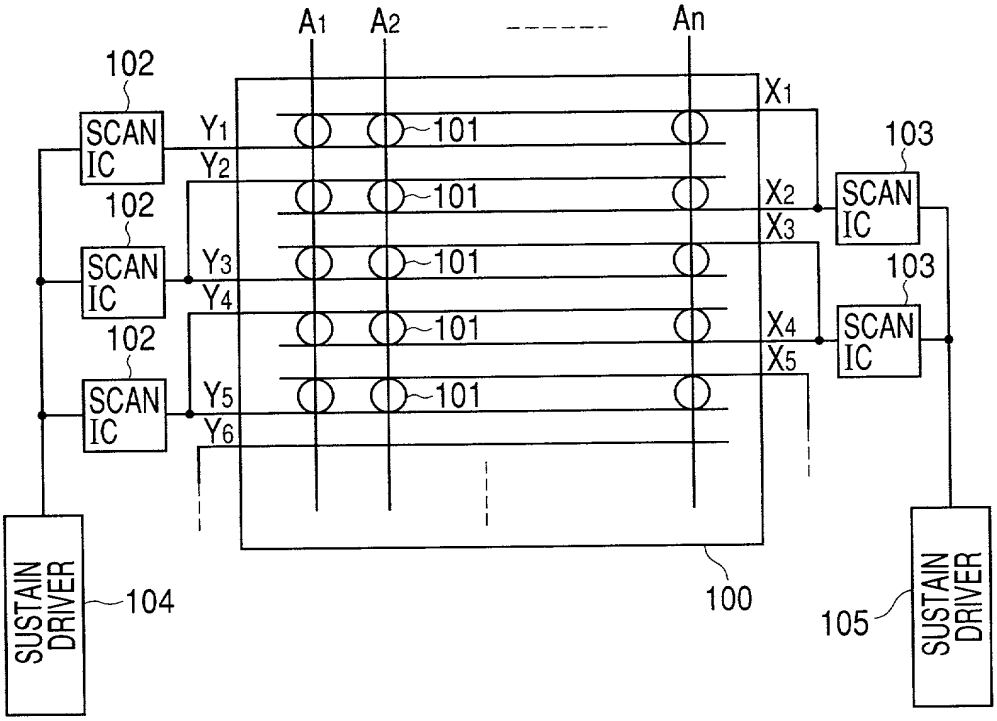

A1
A2
An
102
SCAN IC
Y1
Y2
Y3
Y4
Y5
Y6
101
X1
X2
X3
X4
X5
103
SCAN IC
SUSTAIN DRIVER
104
105
100

FIG. 10

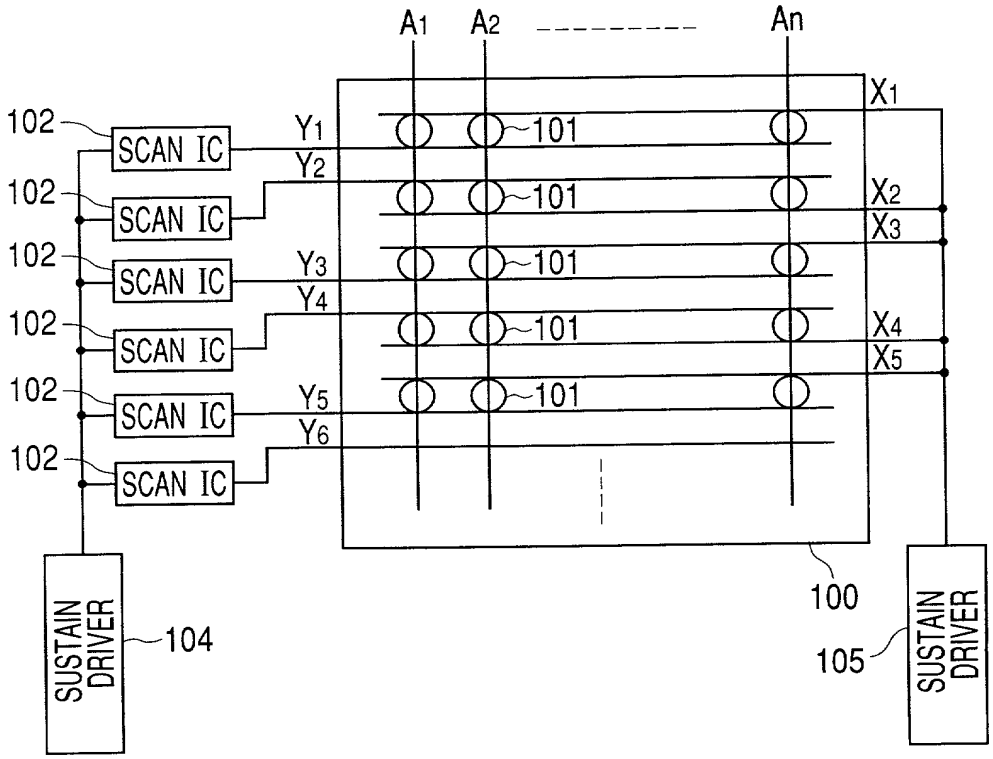

A1
A2
An
X1
X2
X3
X4
X5
Y1
Y2
Y3
Y4
Y5
Y6
101
102
SCAN IC
SUSTAIN DRIVER
104
105
100

FIG. 11

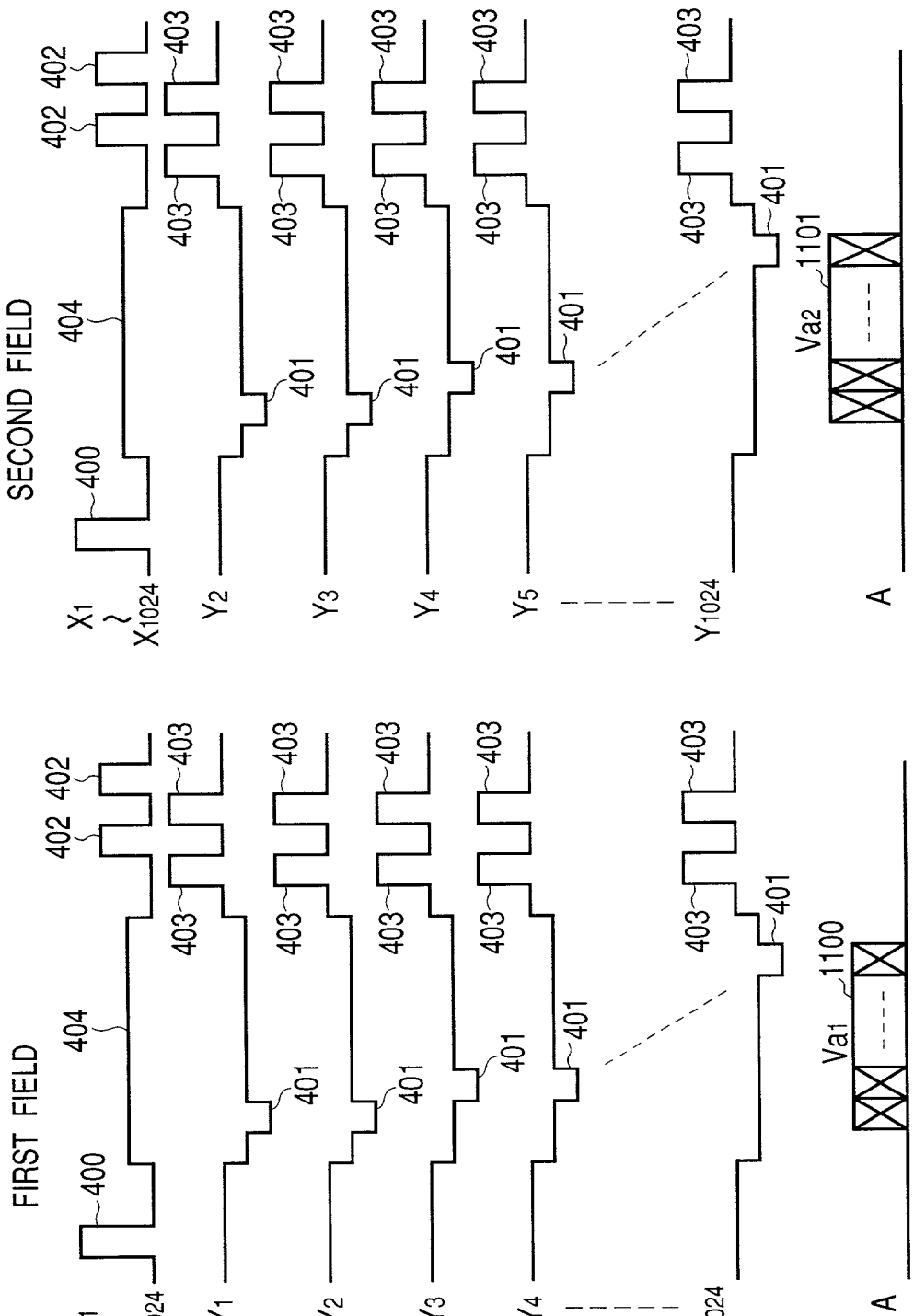

FIRST FIELD
SECOND FIELD
X1
X1024
Y1
Y2
Y3
Y4
Y5
Y1024
A
400
401
402
403
404
1100
1101
Va1
Va2

FIG. 12

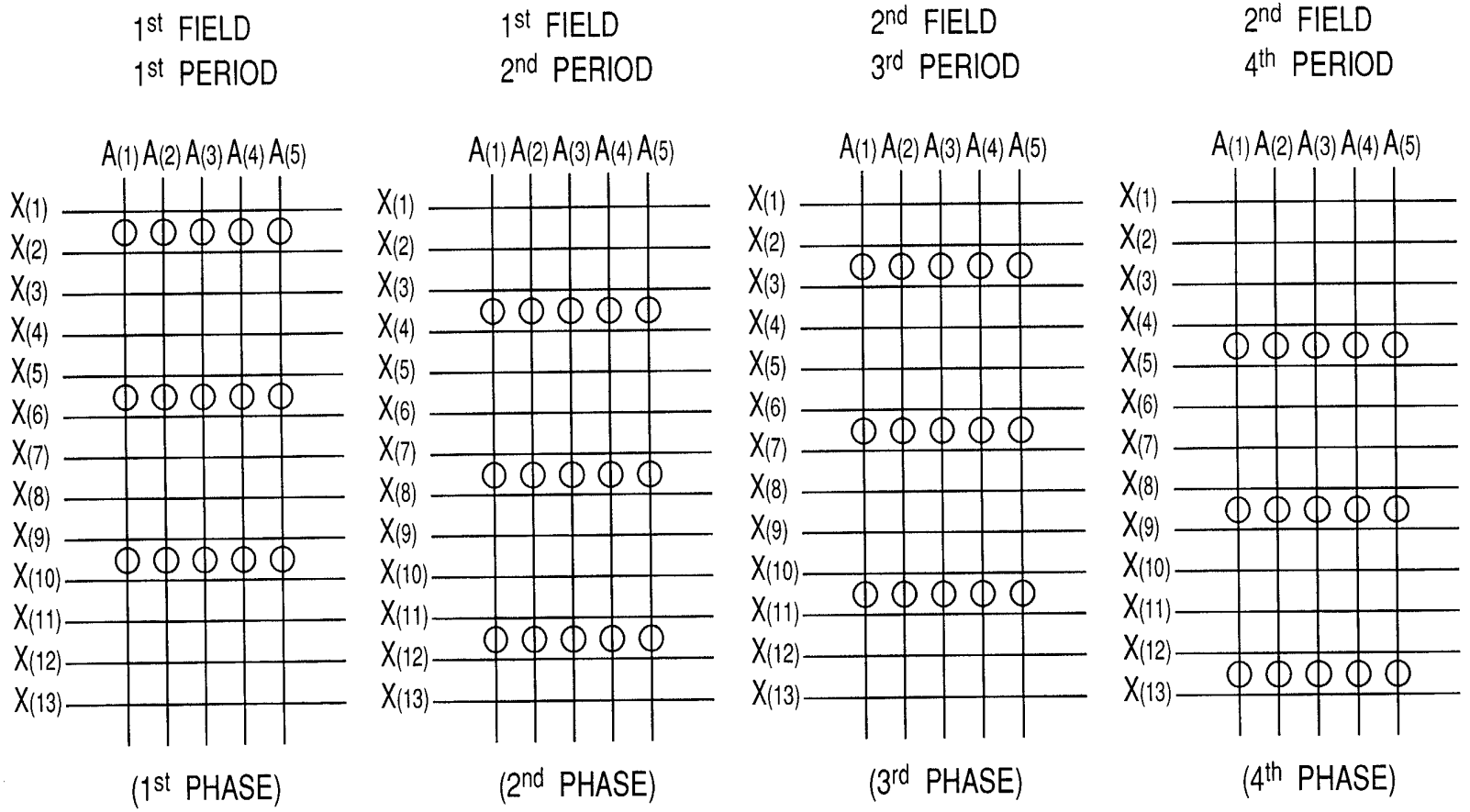


FIG. 13

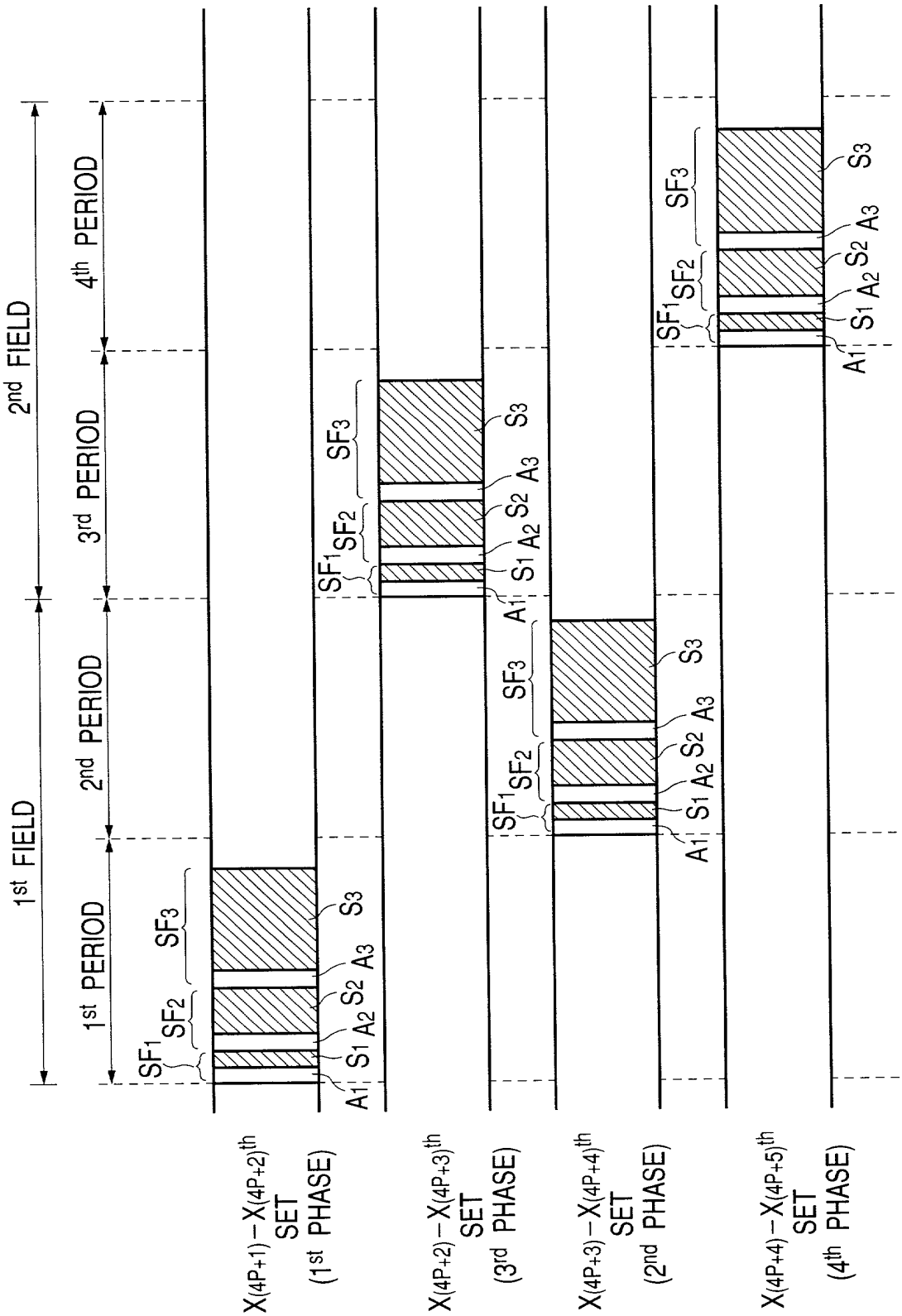

1st FIELD
2nd FIELD
1st PERIOD
2nd PERIOD
3rd PERIOD
4th PERIOD
SF1
SF2
SF3
A1
S1
A2
S2
A3
S3
X(4P+1)−X(4P+2)th SET (1st PHASE)
X(4P+2)−X(4P+3)th SET (3rd PHASE)
X(4P+3)−X(4P+4)th SET (2nd PHASE)
X(4P+4)−X(4P+5)th SET (4th PHASE)

FIG. 14

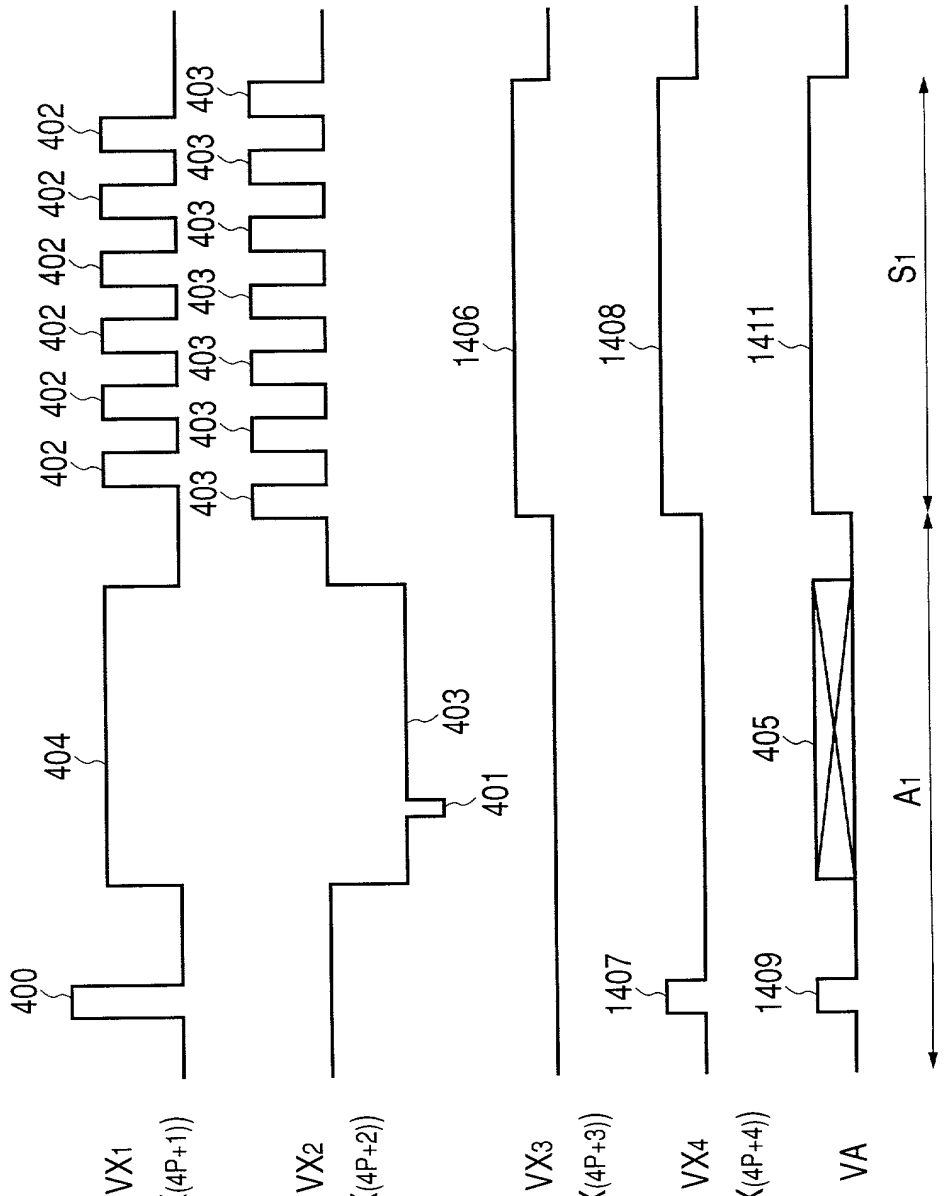

VX1
(X(4P+1))
VX2
(X(4P+2))
VX3
(X(4P+3))
VX4
(X(4P+4))
VA
400
404
402
403
401
1406
1407
1408
1409
1411
405
A1
S1

FIG. 15

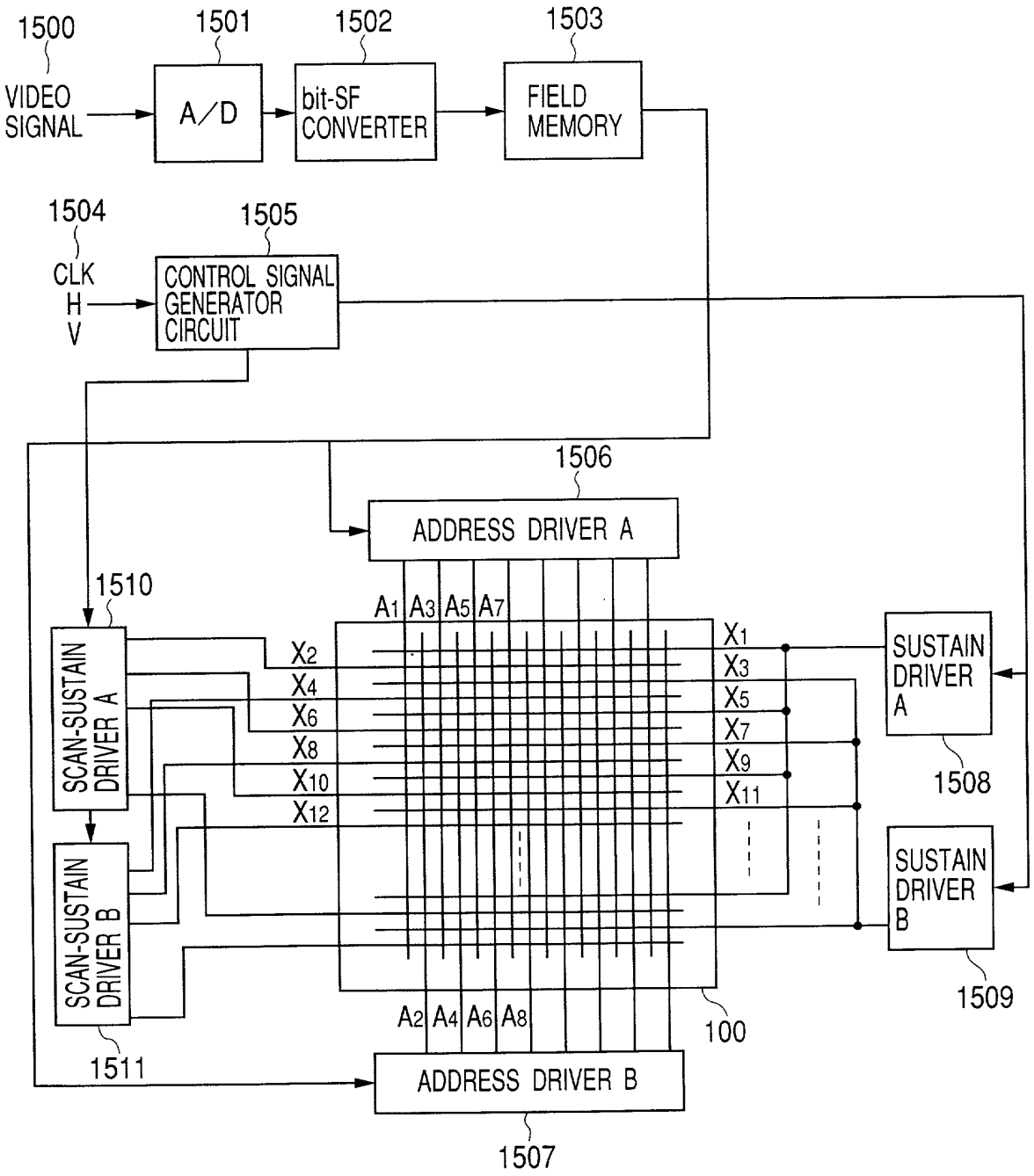

1500
VIDEO SIGNAL
1501
A/D
1502
bit-SF CONVERTER
1503
FIELD MEMORY
1504
CLK
H
V
1505
CONTROL SIGNAL GENERATOR CIRCUIT
1506
ADDRESS DRIVER A
1510
SCAN-SUSTAIN DRIVER A
SCAN-SUSTAIN DRIVER B
1511
A1 A3 A5 A7
A2 A4 A6 A8
X1 X2 X3 X4 X5 X6 X7 X8 X9 X10 X11 X12
100
SUSTAIN DRIVER A
1508
SUSTAIN DRIVER B
1509
ADDRESS DRIVER B
1507

FIG. 16

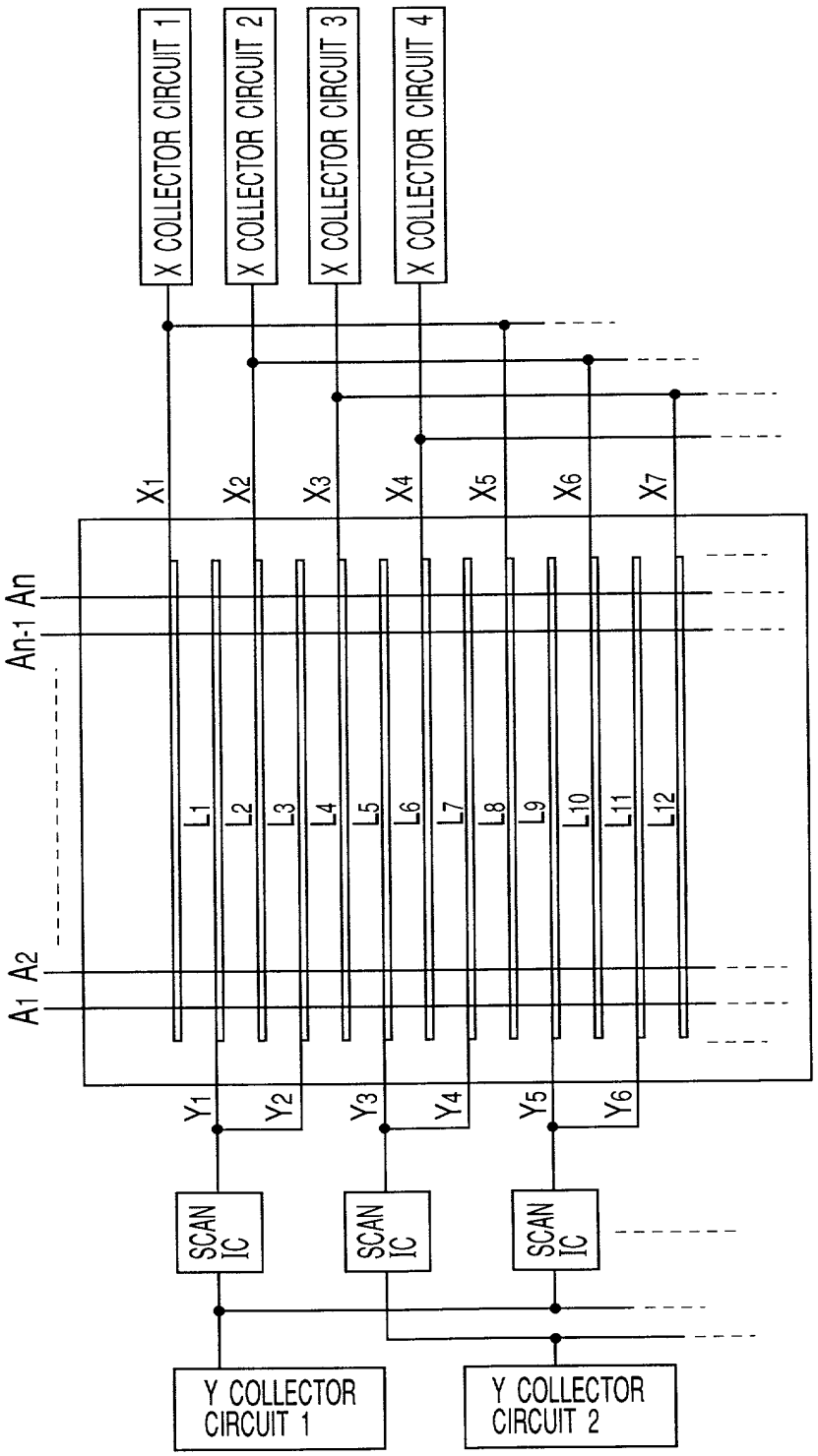

X COLLECTOR CIRCUIT 1
X COLLECTOR CIRCUIT 2
X COLLECTOR CIRCUIT 3
X COLLECTOR CIRCUIT 4
X1
X2
X3
X4
X5
X6
X7
An
An-1
A2
A1
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
Y1
Y2
Y3
Y4
Y5
Y6
SCAN IC
SCAN IC
SCAN IC
Y COLLECTOR CIRCUIT 1
Y COLLECTOR CIRCUIT 2

FIG. 17

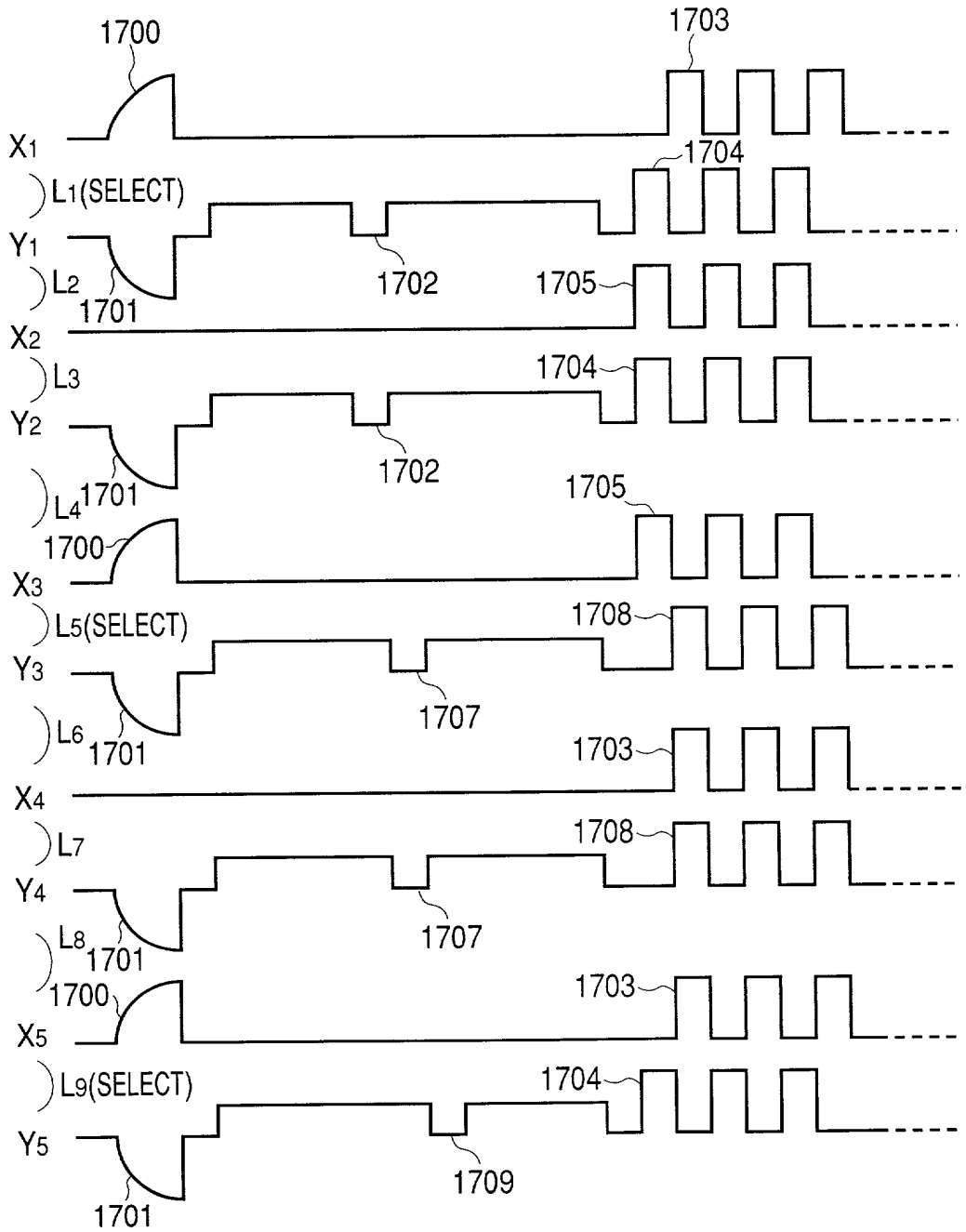

1700
1703
X1
1704
L1(SELECT)
Y1
L2
1701
1702
1705
X2
L3
1704
Y2
1702
L4
1701
1705
1700
X3
L5(SELECT)
1708
Y3
1707
L6
1701
1703
X4
L7
1708
Y4
1707
L8
1701
1700
1703
X5
L9(SELECT)
1704
Y5
1709
1701

FIG. 18

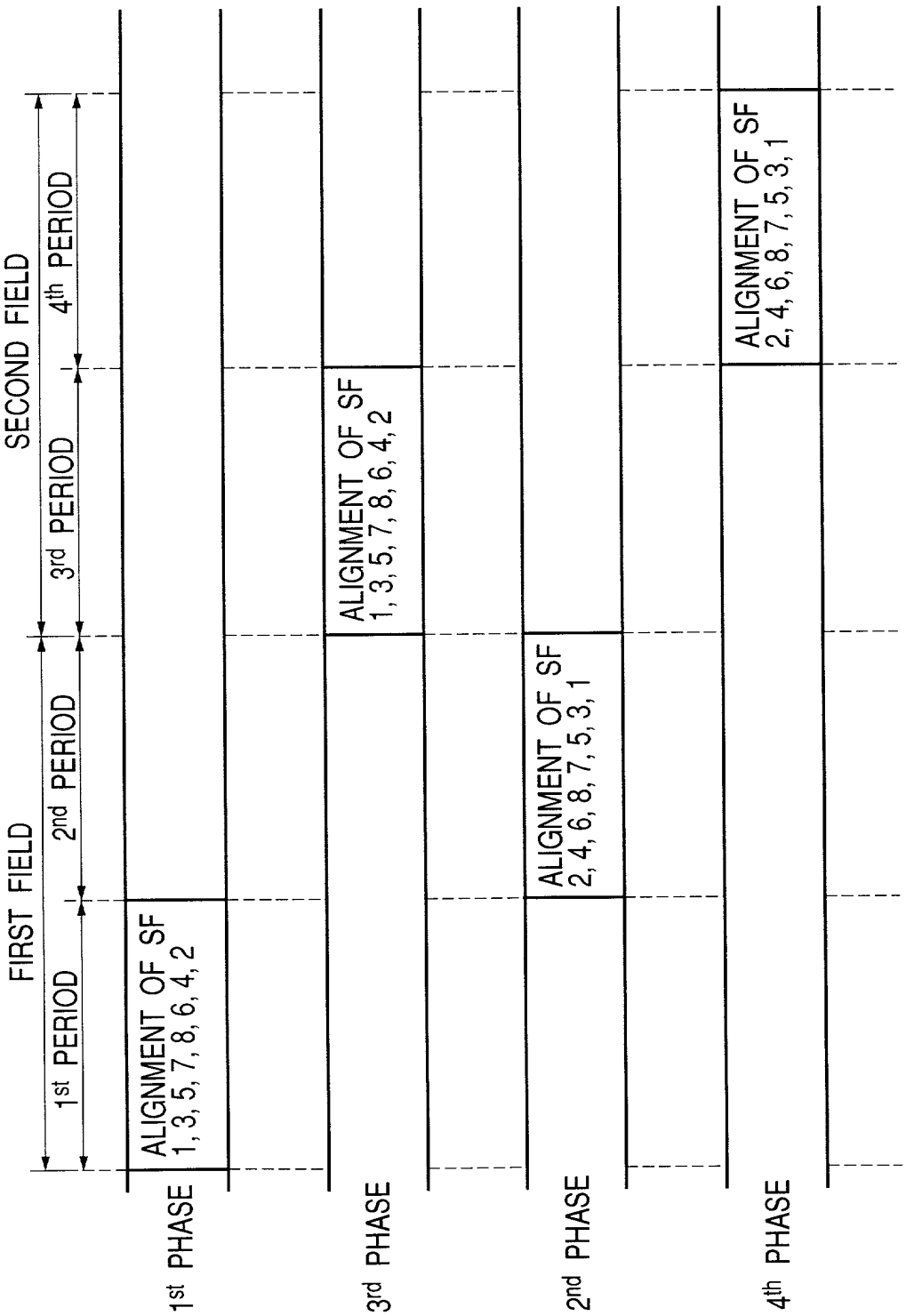

FIRST FIELD
SECOND FIELD
1st PERIOD
2nd PERIOD
3rd PERIOD
4th PERIOD
1st PHASE
ALIGNMENT OF SF
1, 3, 5, 7, 8, 6, 4, 2
3rd PHASE
ALIGNMENT OF SF
1, 3, 5, 7, 8, 6, 4, 2
2nd PHASE
ALIGNMENT OF SF
2, 4, 6, 8, 7, 5, 3, 1
4th PHASE
ALIGNMENT OF SF
2, 4, 6, 8, 7, 5, 3, 1

FIG. 19

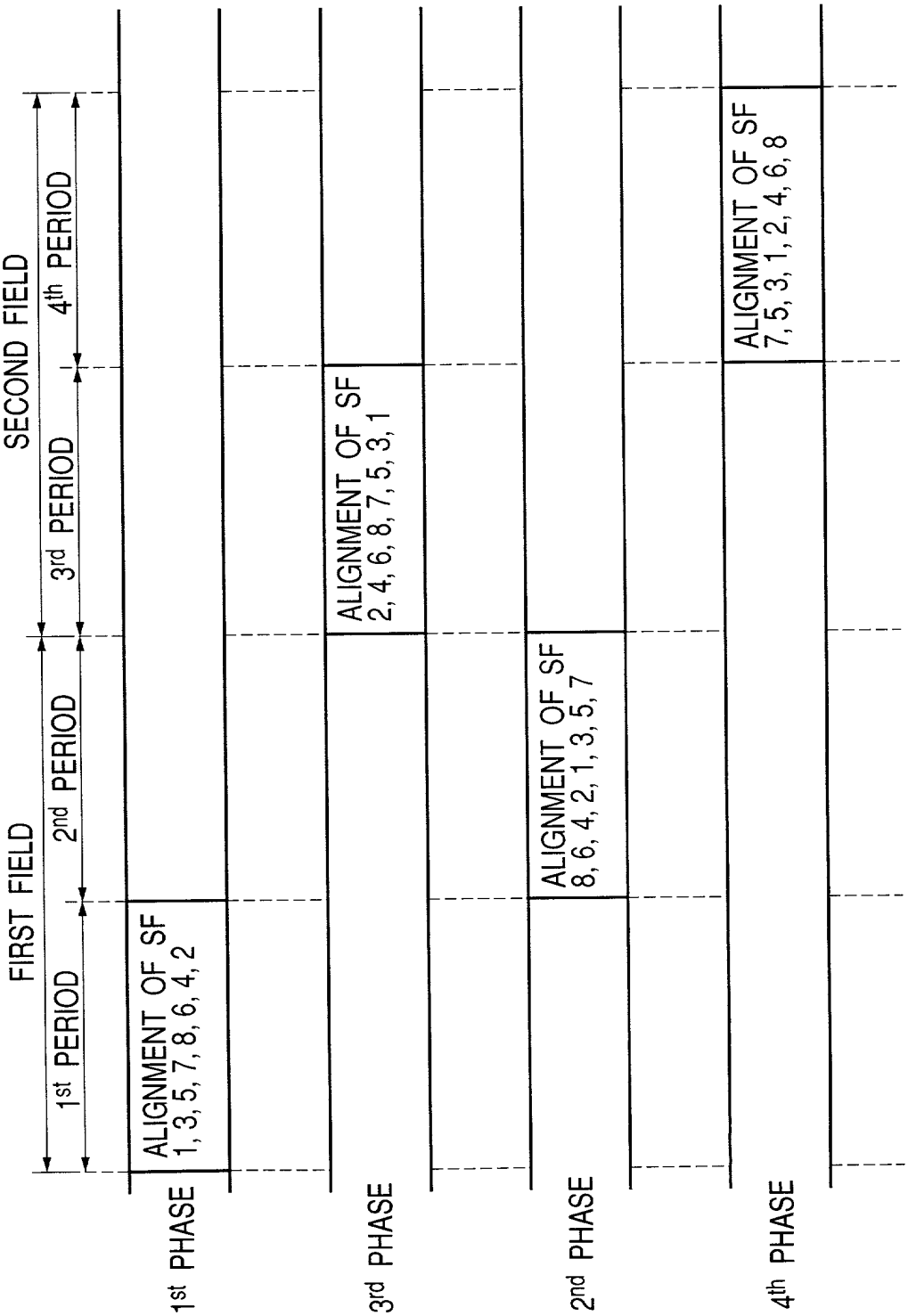

FIRST FIELD
SECOND FIELD
1st PERIOD
2nd PERIOD
3rd PERIOD
4th PERIOD
1st PHASE
ALIGNMENT OF SF
1, 3, 5, 7, 8, 6, 4, 2
3rd PHASE
ALIGNMENT OF SF
2, 4, 6, 8, 7, 5, 3, 1
2nd PHASE
ALIGNMENT OF SF
8, 6, 4, 2, 1, 3, 5, 7
4th PHASE
ALIGNMENT OF SF
7, 5, 3, 1, 2, 4, 6, 8

FIG. 20

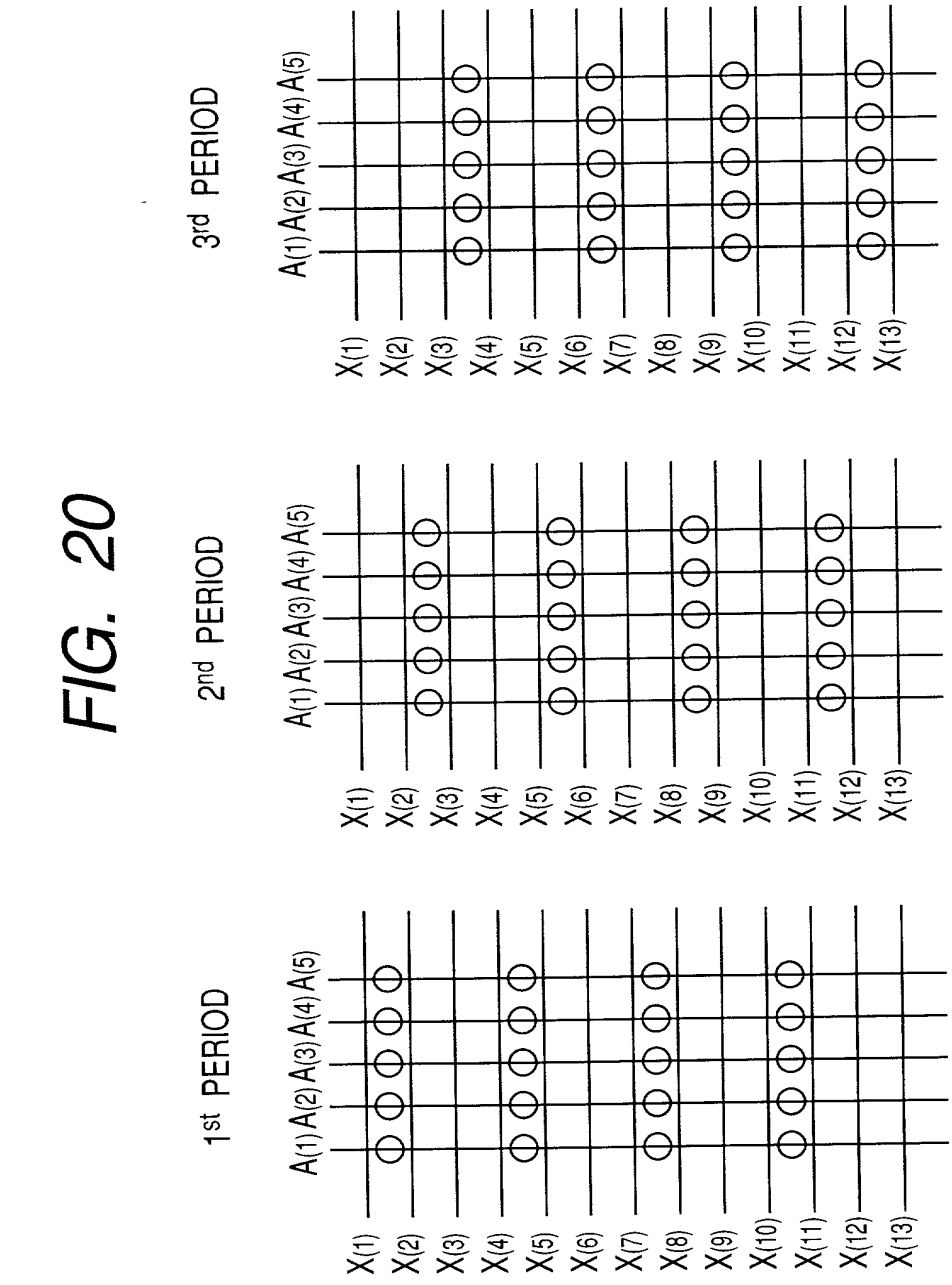

1st PERIOD
2nd PERIOD
3rd PERIOD
A(1) A(2) A(3) A(4) A(5)
X(1)
X(2)
X(3)
X(4)
X(5)
X(6)
X(7)
X(8)
X(9)
X(10)
X(11)
X(12)
X(13)

FIG. 21

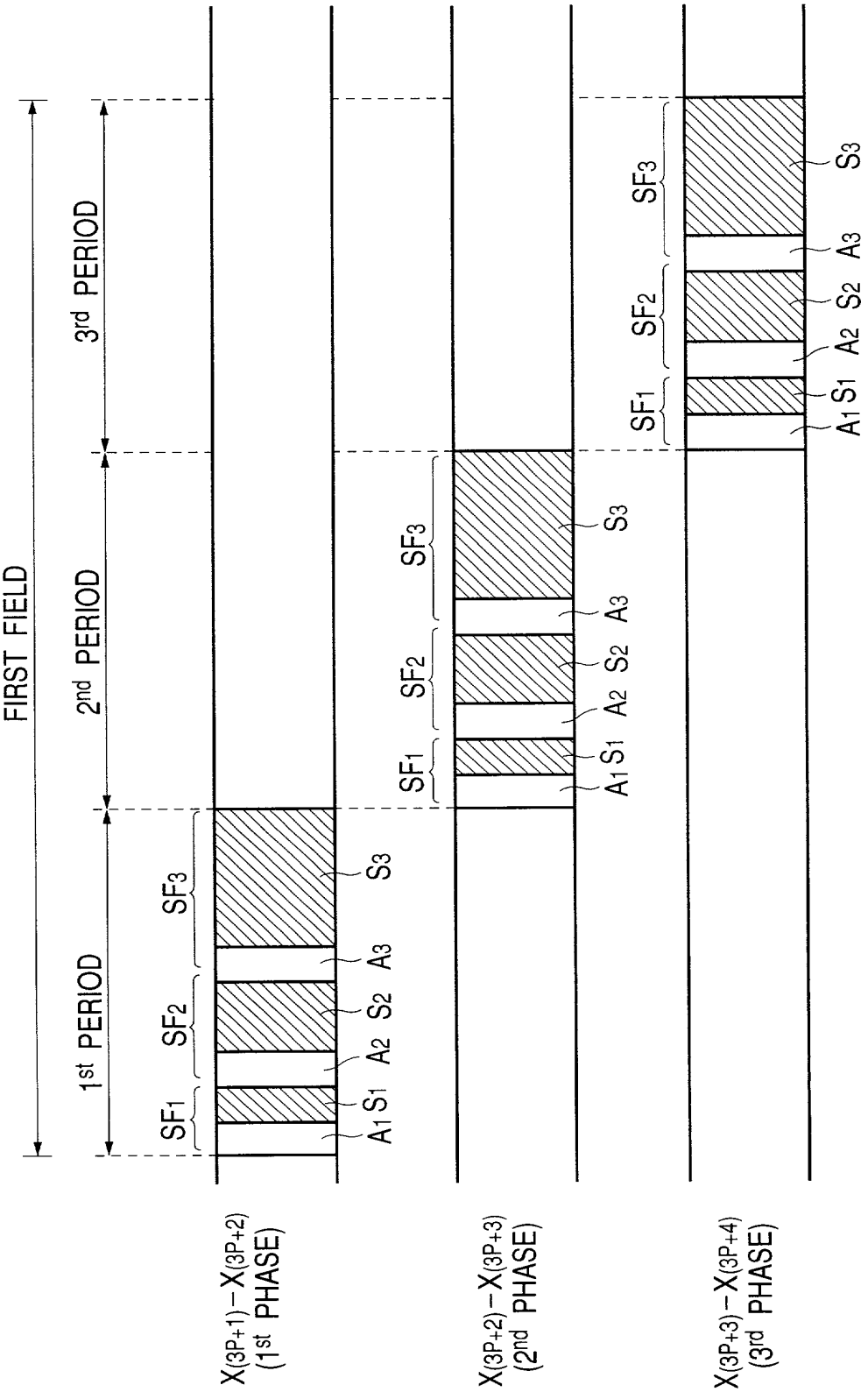

FIRST FIELD
1st PERIOD
2nd PERIOD
3rd PERIOD
SF1
SF2
SF3
A1 S1 A2 S2 A3 S3
X(3P+1) – X(3P+2)
(1st PHASE)
X(3P+2) – X(3P+3)
(2nd PHASE)
X(3P+3) – X(3P+4)
(3rd PHASE)

FIG. 22

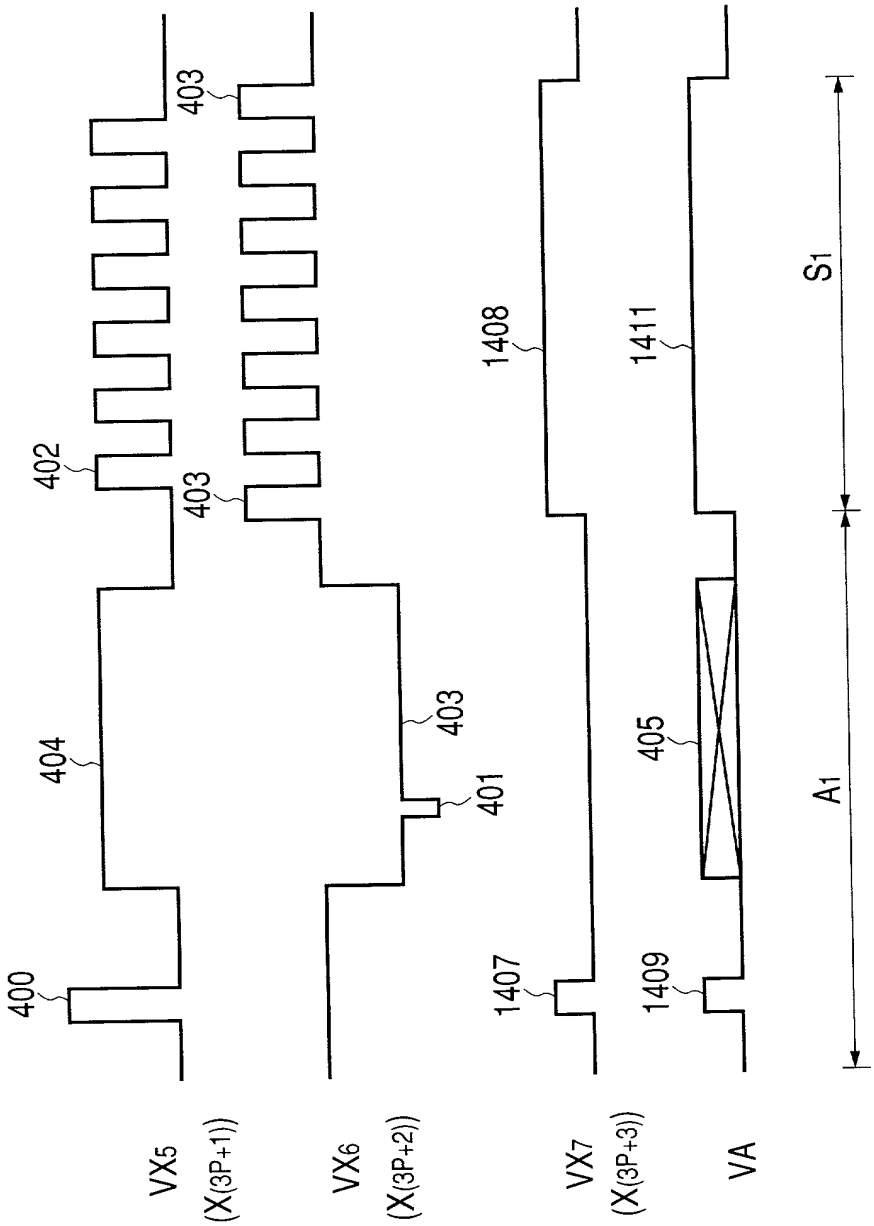

400
404
402
403
403
VX5
(X(3P+1))
403
401
VX6
(X(3P+2))
1408
1407
VX7
(X(3P+3))
1411
1409
405
VA
S1
A1

FIG. 23

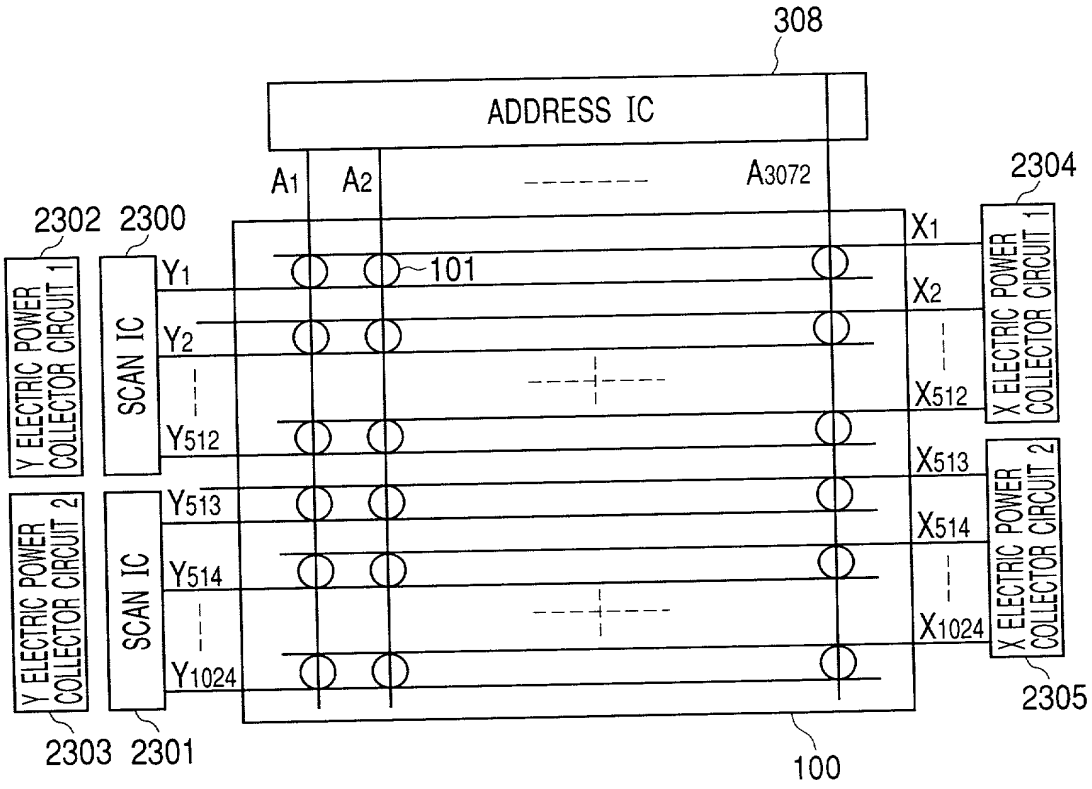

308
ADDRESS IC
A1
A2
A3072
2304
2302
2300
Y ELECTRIC POWER COLLECTOR CIRCUIT 1
SCAN IC
Y1
Y2
Y512
101
X1
X2
X512
X ELECTRIC POWER COLLECTOR CIRCUIT 1
Y ELECTRIC POWER COLLECTOR CIRCUIT 2
SCAN IC
Y513
Y514
Y1024
X513
X514
X1024
X ELECTRIC POWER COLLECTOR CIRCUIT 2
2305
2303
2301
100

FIG. 24

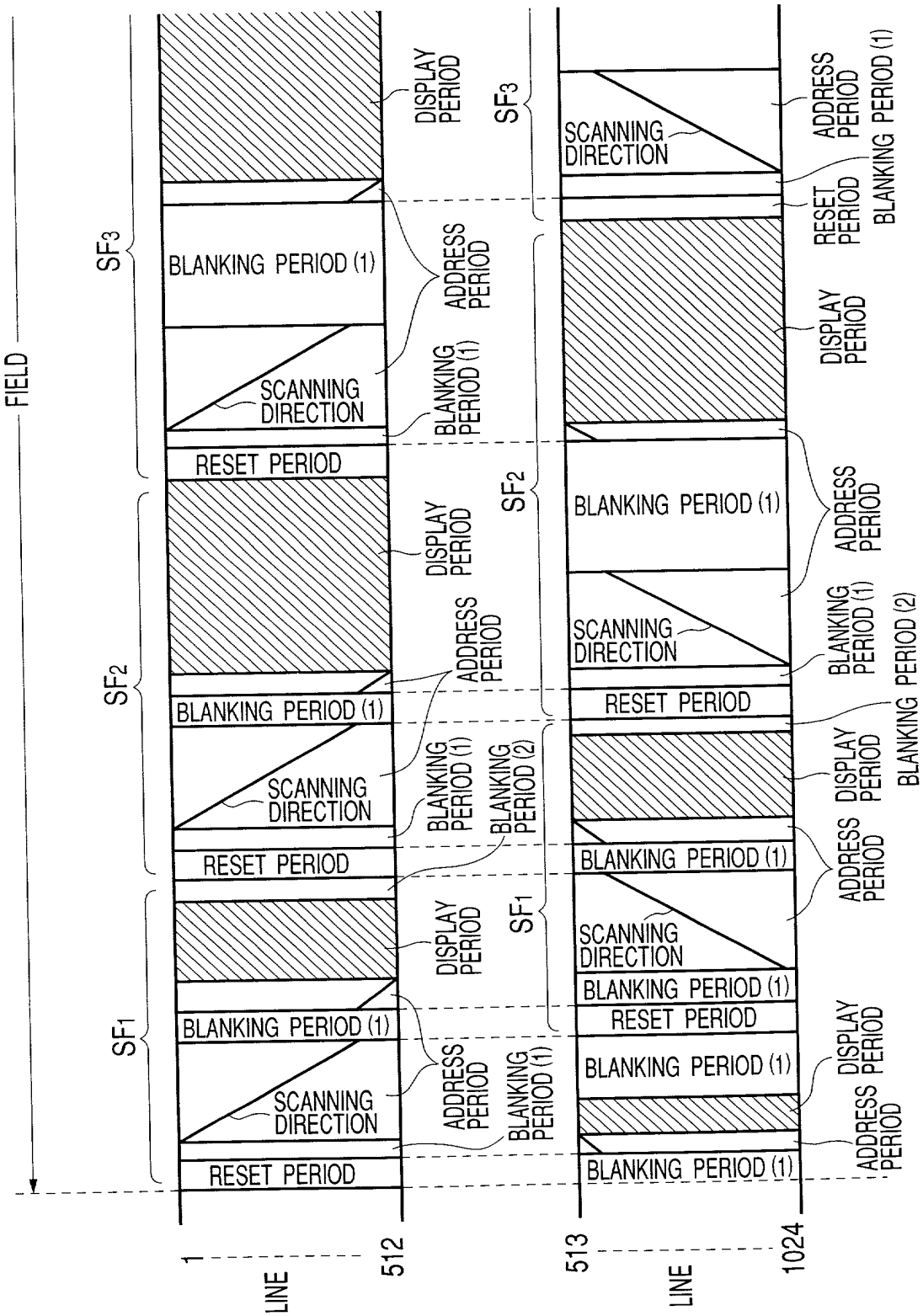

FIELD
SF3
SF2
SF1
DISPLAY PERIOD
BLANKING PERIOD (1)
ADDRESS PERIOD
SCANNING DIRECTION
RESET PERIOD
BLANKING PERIOD (2)
1
512
513
1024
LINE

FIG. 25

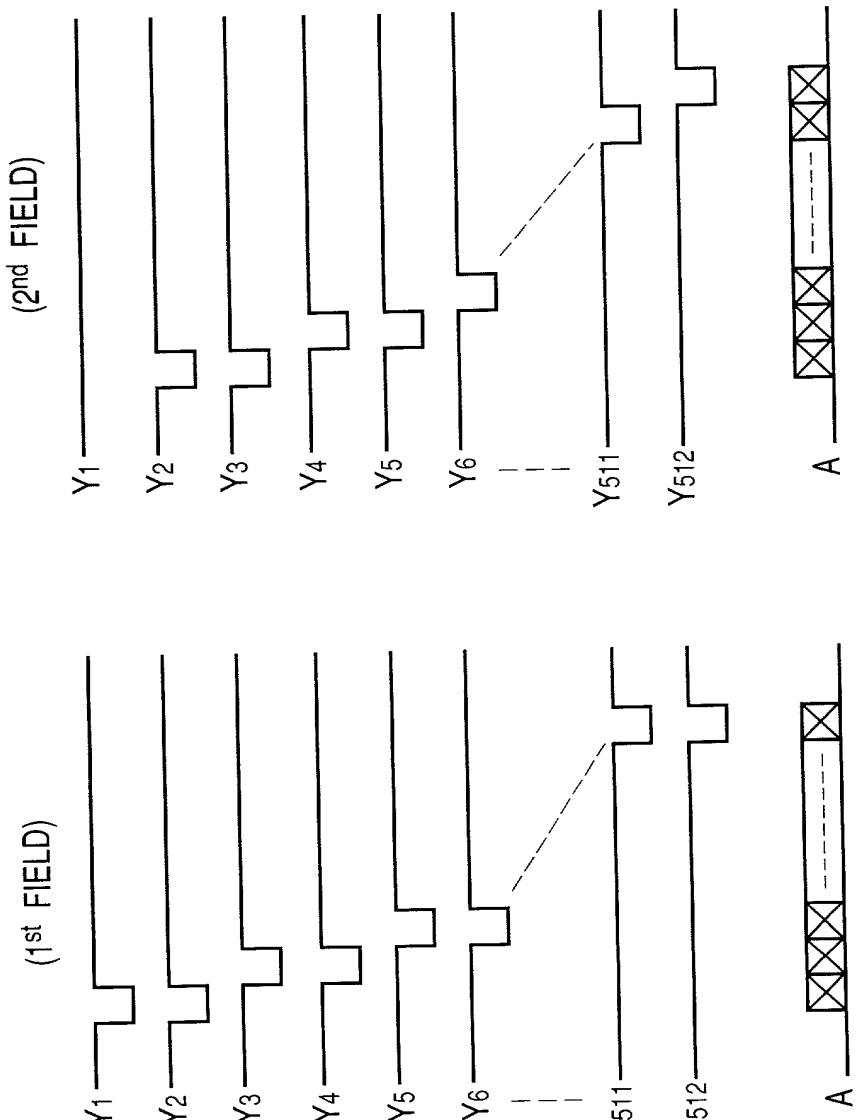


FIG. 26

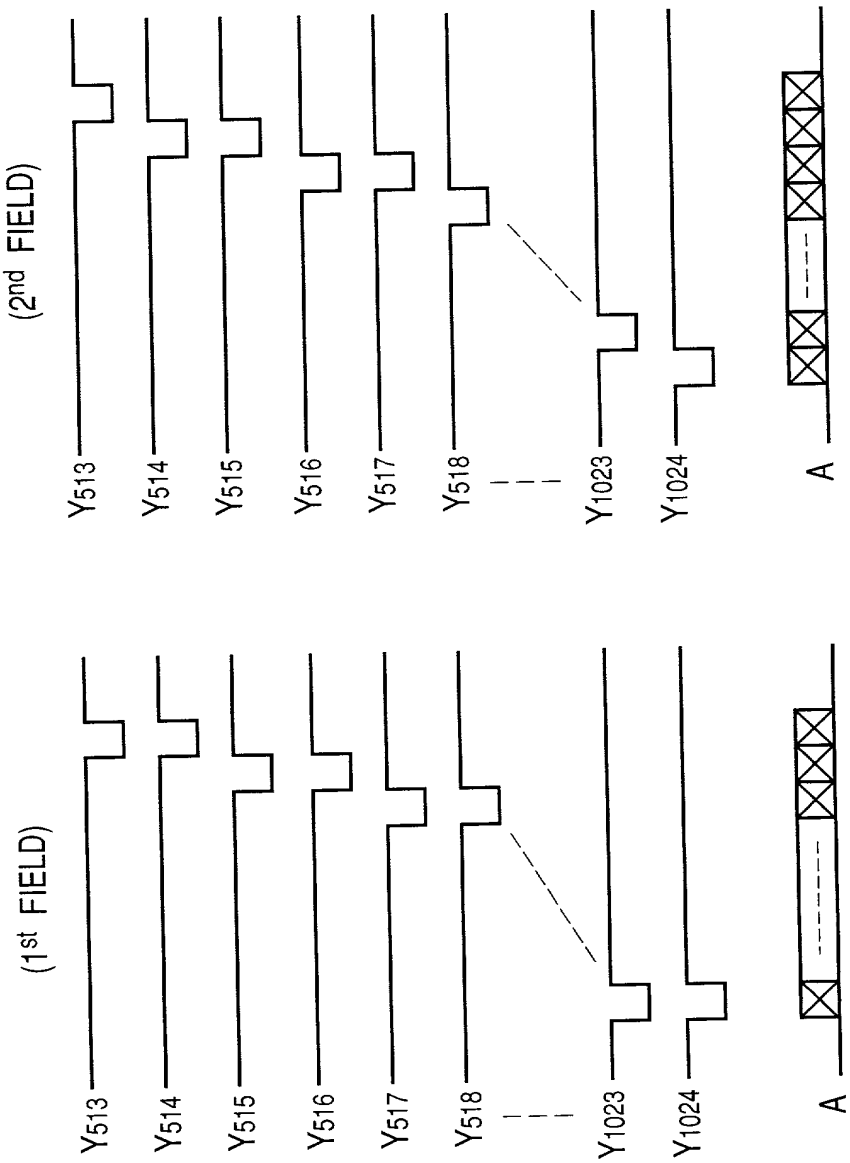

(1st FIELD)
(2nd FIELD)
Y513
Y514
Y515
Y516
Y517
Y518
Y1023
Y1024
A

FIG. 27

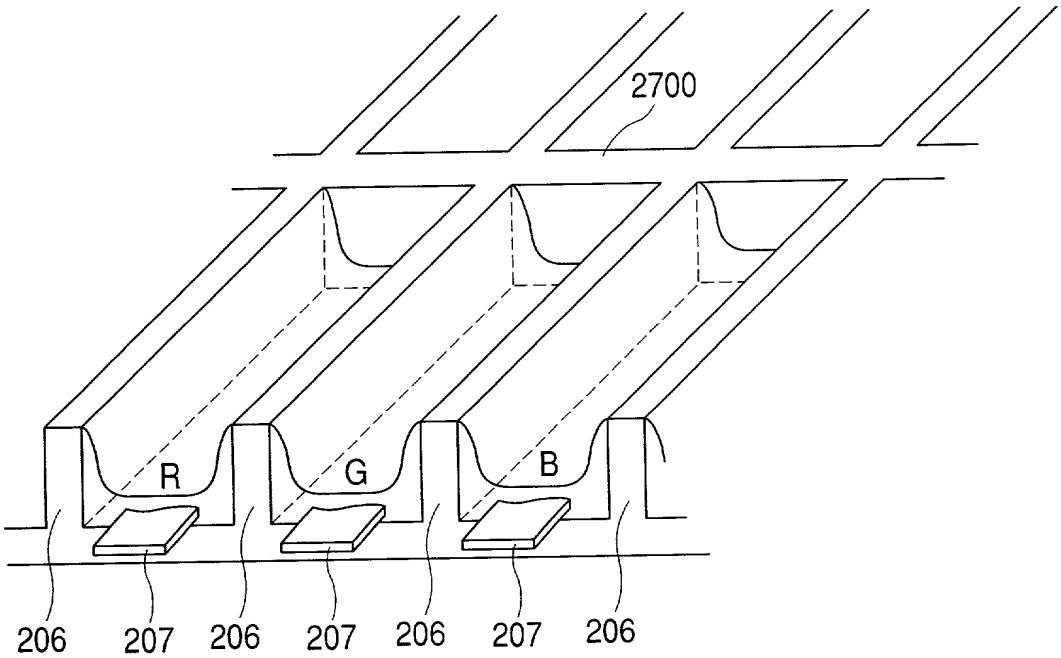


FIG. 28

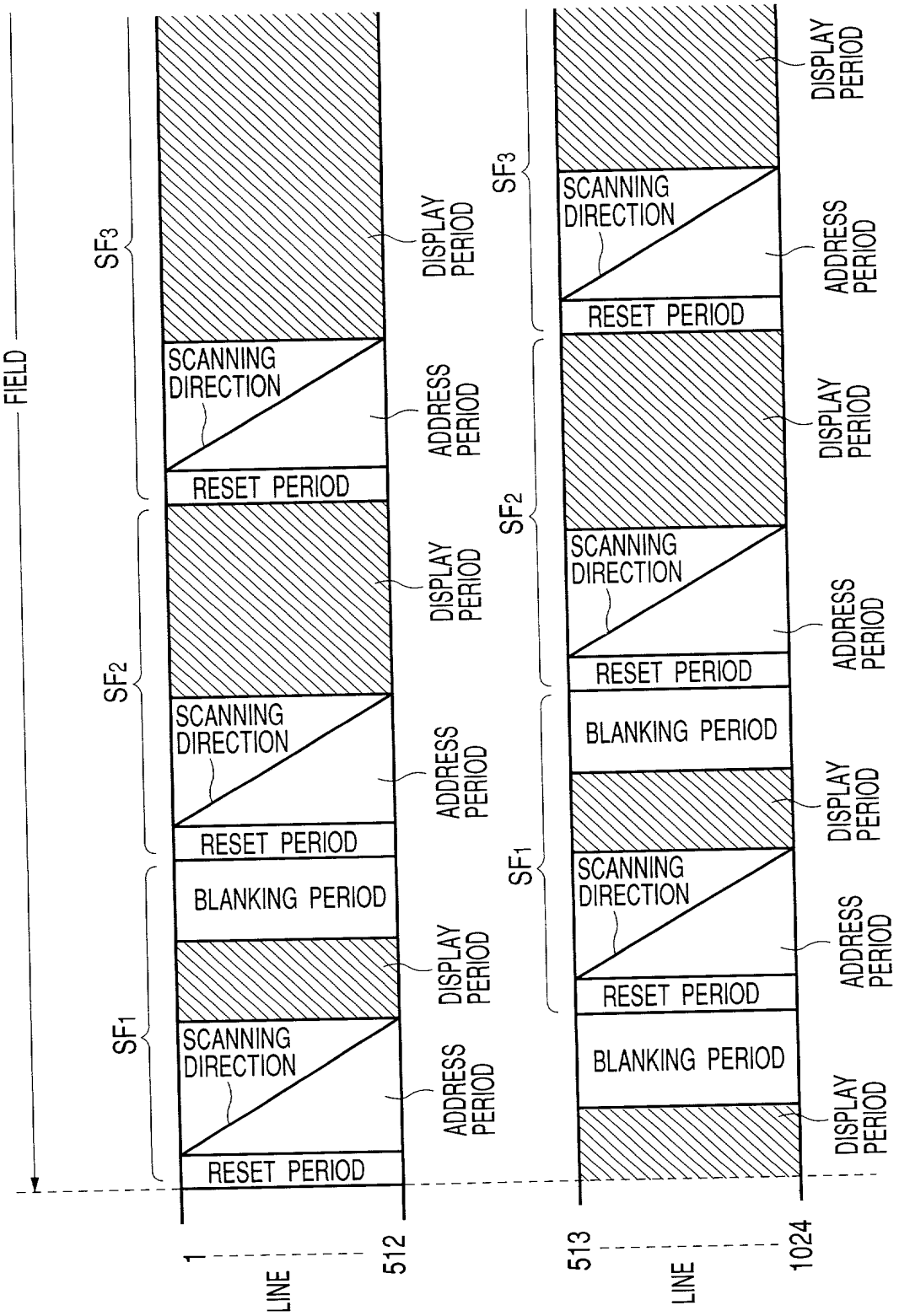
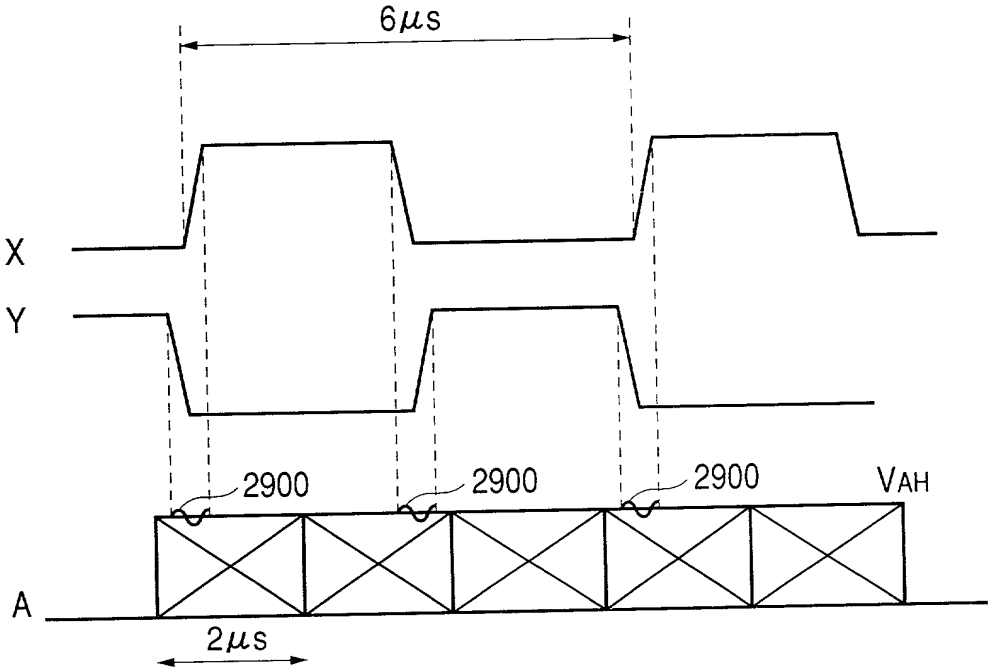

FIELD
SF3
SF2
SF1
SCANNING DIRECTION
ADDRESS PERIOD
RESET PERIOD
DISPLAY PERIOD
BLANKING PERIOD
1
512
513
1024
LINE

FIG. 29

(a)


6μs
X
Y
2900
2900
2900
VAH
A
2μs

(b)

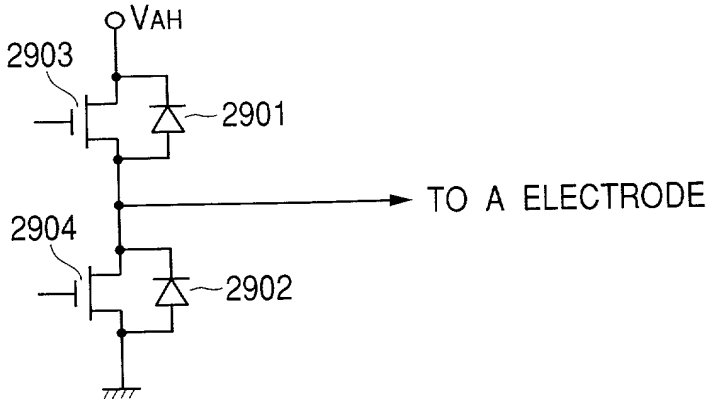

VAH
2903
2901
TO A ELECTRODE
2904
2902

FIG. 30

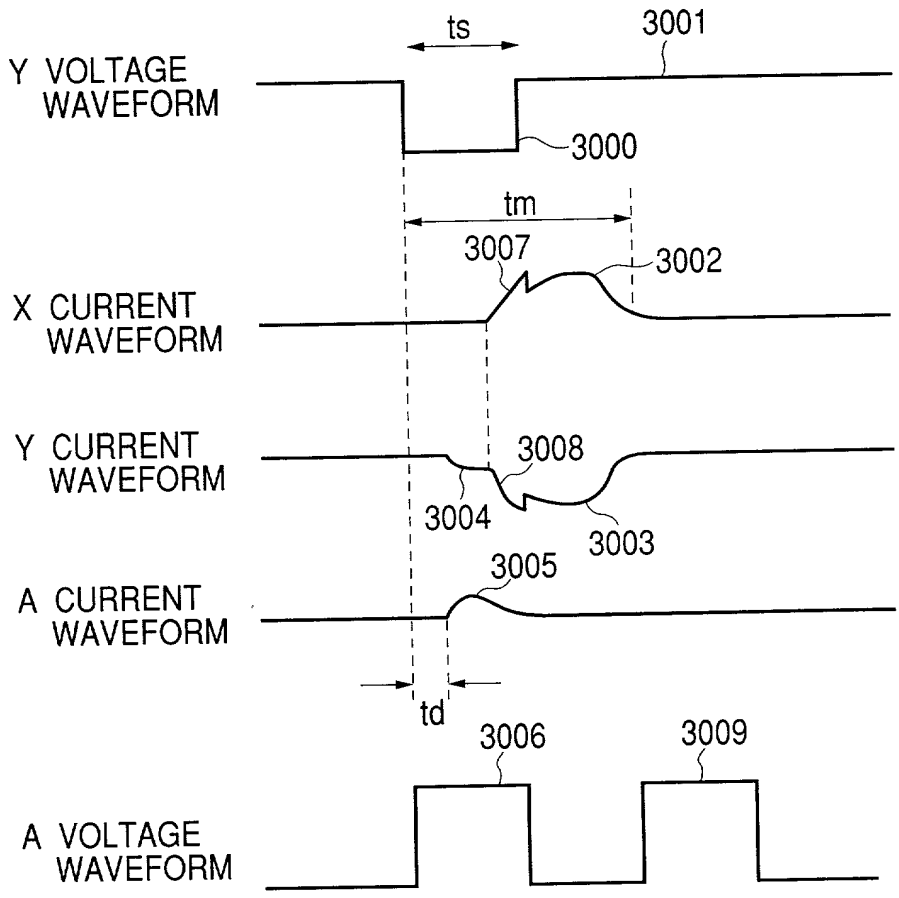

ts
3001
Y VOLTAGE WAVEFORM
3000
tm
3007
3002
X CURRENT WAVEFORM
Y CURRENT WAVEFORM
3008
3004
3003
3005
A CURRENT WAVEFORM
td
3006
3009
A VOLTAGE WAVEFORM

FIG. 31

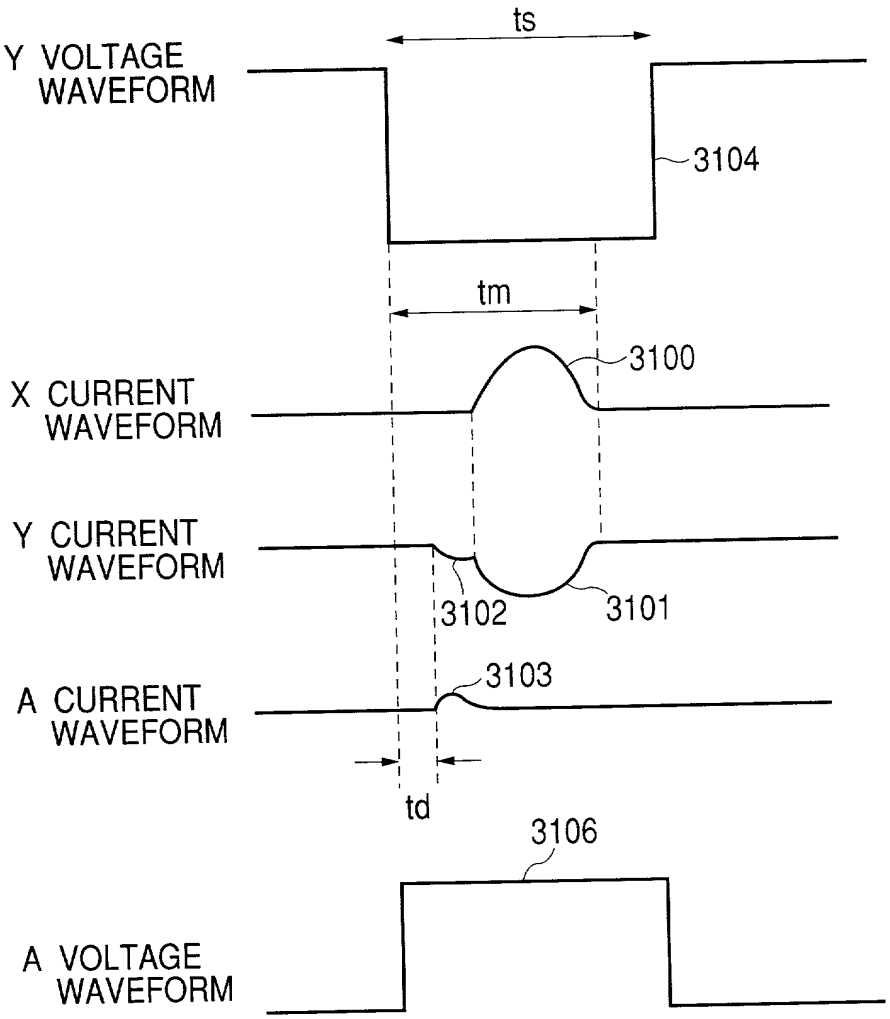

ts
Y VOLTAGE WAVEFORM
3104
tm
3100
X CURRENT WAVEFORM
Y CURRENT WAVEFORM
3102
3101
3103
A CURRENT WAVEFORM
td
3106
A VOLTAGE WAVEFORM

FIG. 32

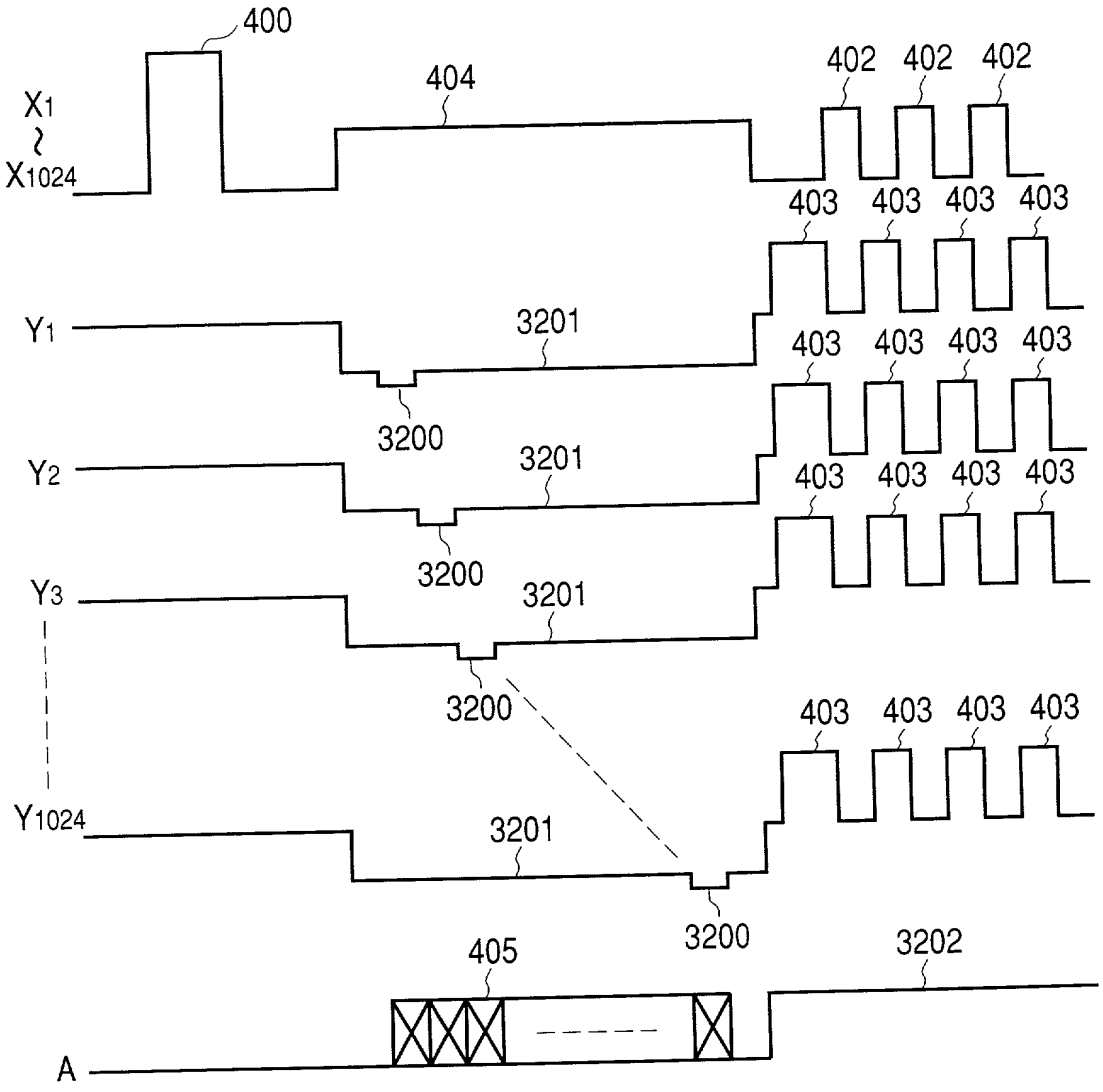
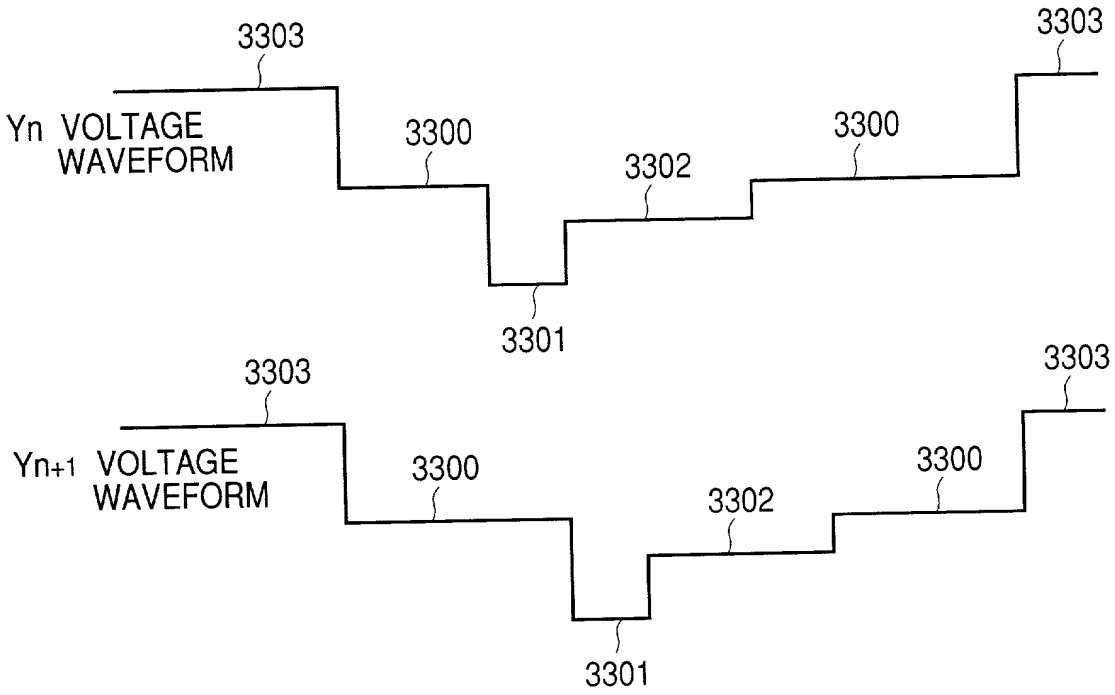

400
404
402 402 402
X1
X1024
403 403 403 403
Y1
3201
3200
403 403 403 403
Y2
3201
3200
403 403 403 403
Y3
3201
3200
403 403 403 403
Y1024
3201
3200
405
3202
A

FIG. 33


3303
3303
Yn VOLTAGE WAVEFORM
3300
3300
3302
3301
3303
3303
Yn+1 VOLTAGE WAVEFORM
3300
3300
3302
3301

NT0442

PTO/SB/106(8-96)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DISPLAY AND IMAGE DISPLAYING METHOD

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on March 19, 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/01400 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106(8-96)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106(8-96) (Modulated spacing)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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発明者の署名 日付	*Inventor's signature* Date Akihiko Kougami 7/30/2001
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(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者	2-00	Full name of second joint inventor, if any Kazutaka NAKA
第二共同発明者の署名 日付	Kazutaka Naka	Second inventor's signature Date 7/6/2001
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第三共同発明者の署名 日付	Hiroshi Ohtaka	Third inventor's signature Date 7/9/2001
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第四共同発明者の署名 日付	Michitaka Ohsawa	Fourth inventor's signature Date 7/9/2001
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第五共同発明者		Full name of fifth joint inventor, if any
第五共同発明者の署名 日付		Fifth inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and subsequent joint inventors.)

第六共同発明者	Full name of sixth joint inventor, if any
第六共同発明者の署名　日付	Sixth inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address
第七共同発明者	Full name of seventh joint inventor, if any
第七共同発明者の署名　日付	Seventh inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address
第八共同発明者	Full name of eighth joint inventor, if any
第八共同発明者の署名　日付	Eighth inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address
第九共同発明者	Full name of ninth joint inventor, if any
第九共同発明者の署名　日付	Ninth inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

(第十以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for tenth and subsequent joint inventors.)